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Citation Report

#	ARTICLE	IF	CITATIONS
1	A Vision for All-Spin Neural Networks: A Device to System Perspective. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 2267-2277.	3.5	58
2	Fathom: reference workloads for modern deep learning methods. , 2016, , .		96
3	Utilizing 3D ICs in architectures for neural networks. , 2016, , .		0
4	IMEC: A Fully Morphable In-Memory Computing Fabric Enabled by Resistive Crossbar. IEEE Computer Architecture Letters, 2017, 16, 123-126.	1.0	6
5	DLPlib: A Library for Deep Learning Processor. Journal of Computer Science and Technology, 2017, 32, 286-296.	0.9	5
6	Processing-In-Memory Architecture Design for Accelerating Neuro-Inspired Algorithms. , 2017, , 183-207.		1
7	A generalized model of TiO _x -based memristive devices and its application for image processing. Chinese Physics B, 2017, 26, 090502.	0.7	6
8	MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, , 1-1.	1.9	42
9	Data-centric computation mode for convolution in deep neural networks. , 2017, , .		3
10	Efficient Processing of Deep Neural Networks: A Tutorial and Survey. Proceedings of the IEEE, 2017, 105, 2295-2329.	16.4	2,217
11	Moonwalk. ACM SIGPLAN Notices, 2017, 52, 511-526.	0.2	3
12	TETRIS. Computer Architecture News, 2017, 45, 751-764.	2.5	47
13	Methods for high resolution programming in lithium niobate memristors for neuromorphic hardware. , 2017, , .		3
14	Speeding up crossbar resistive memory by exploiting in-memory data patterns. , 2017, , .		15
15	AEP: An error-bearing neural network accelerator for energy efficiency and model protection. , 2017, , .		2
16	RRAM-based reconfigurable in-memory computing architecture with hybrid routing. , 2017, , .		1
17	Energy Efficient In-Memory Binary Deep Neural Network Accelerator with Dual-Mode SOT-MRAM. , 2017, , .		22
18	High performance and energy-efficient in-memory computing architecture based on SOT-MRAM. , 2017, , .		10

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20	An energy-efficient and high-throughput bitwise CNN on sneak-path-free digital ReRAM crossbar. , 2017, , .		17
21	AEP: An error-bearing neural network accelerator for energy efficiency and model protection. , 2017, , .		1
22	Generalize or Die: Operating Systems Support for Memristor-Based Accelerators. , 2017, , .		7
23	Memristor crossbar based implementation of a multilayer perceptron. , 2017, , .		9
24	AEPE: An area and power efficient RRAM crossbar-based accelerator for deep CNNs. , 2017, , .		20
25	Blurring the Lines between Memory and Computation. IEEE Micro, 2017, 37, 13-15.	1.8	4
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27	TETRIS. , 2017, , .		255
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29	TETRIS. Operating Systems Review (ACM), 2017, 51, 751-764.	1.5	24
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57	A peripheral circuit reuse structure integrated with a retimed data flow for low power RRAM crossbar-based CNN. , 2018, , .		10
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124	Application Codesign of Near-Data Processing for Similarity Search. , 2018, , .		15
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