Eyeriss: An Energy-Efficient Reconfigurable Accelerator Networks

IEEE Journal of Solid-State Circuits

52, 127-138

DOI: 10.1109/jssc.2016.2616357

Citation Report

#	Article	IF	Citations
1	A 5.5GHz 0.84TOPS/mm² neural network engine with stream architecture and resonant clock mesh. , 2016, , .		0
2	Cognitive computation and communication: A complement solution to cloud for IoT. , 2016, , .		1
3	Approximated Prediction Strategy for Reducing Power Consumption of Convolutional Neural Network Processor. , 2016, , .		8
4	CNN-MERP: An FPGA-based memory-efficient reconfigurable processor for forward and backward propagation of convolutional neural networks. , 2016, , .		23
5	A 58.6 mW 30 Frames/s Real-Time Programmable Multiobject Detection Accelerator With Deformable Parts Models on Full HD $1920imes 1080$ Videos. IEEE Journal of Solid-State Circuits, 2017, 52, 844-855.	5.4	12
6	On-Chip Networks, Second Edition. Synthesis Lectures on Computer Architecture, 2017, 12, 1-210.	1.3	34
7	An Energy-Scalable Accelerator for Blind Image Deblurring. IEEE Journal of Solid-State Circuits, 2017, 52, 1849-1862.	5.4	4
8	Deep learning with coherent nanophotonic circuits. Nature Photonics, 2017, 11, 441-446.	31.4	1,845
9	Pipelining a triggered processing element. , 2017, , .		11
10	C <scp>ir</scp> CNN. , 2017, , .		141
11	An Introduction to Deep Learning for the Physical Layer. IEEE Transactions on Cognitive Communications and Networking, 2017, 3, 563-575.	7.9	1,788
12	Adaptive and Energy-Efficient Architectures for Machine Learning: Challenges, Opportunities, and Research Roadmap. , 2017, , .		30
13	Hardware for machine learning: Challenges and opportunities. , 2017, , .		111
14	Efficient Processing of Deep Neural Networks: A Tutorial and Survey. Proceedings of the IEEE, 2017, 105, 2295-2329.	21.3	2,217
15	AIScale â€" A coarse grained reconfigurable CNN hardware accelerator. , 2017, , .		2
16	Still a Fight to Get It Right: Verification in the Era of Machine Learning. , 2017, , .		4
17	Transfer learning for sEMG hand gestures recognition using convolutional neural networks. , 2017, , .		107
18	Reducing off-chip memory traffic in deep CNNs using stick buffer cache. , 2017, , .		4

#	Article	IF	Citations
19	Neural networks: Efficient implementations and applications. , 2017, , .		10
20	Accelerating deep learning by binarized hardware. , 2017, , .		2
21	Modified distributed arithmetic based low complexity CNN architecture design methodology. , 2017, , .		12
22	Instruction driven cross-layer CNN accelerator with winograd transformation on FPGA. , 2017, , .		27
23	FPGA implementation of convolutional neural network based on stochastic computing. , 2017, , .		7
24	FPGA-based accelerator for losslessly quantized convolutional neural networks. , 2017, , .		9
25	Designing Hardware for Machine Learning: The Important Role Played by Circuit Designers. IEEE Solid-State Circuits Magazine, 2017, 9, 46-54.	0.4	42
26	A 2.56mm² 718GOPS configurable spiking convolutional sparse coding processor in 40nm CMOS. , 2017, , .		2
27	IP core for efficient zero-run length compression of CNN feature maps. , 2017, , .		3
28	A 21mW low-power recurrent neural network accelerator with quantization tables for embedded deep learning applications. , 2017, , .		13
29	An energy-efficient and high-throughput bitwise CNN on sneak-path-free digital ReRAM crossbar. , 2017, , .		17
30	TensorQuant. , 2017, , .		11
31	Using Fermat number transform to accelerate convolutional neural network. , 2017, , .		6
32	Evolutionary approximation of gradient orientation module in HOG-based human detection system. , 2017, , .		3
33	A novel design of hardware realizable ANN predictor with weight converted multiplication. , 2017, , .		0
34	The Design and Implementation of Scalable Deep Neural Network Accelerator Cores. , 2017, , .		6
35	Towards optimal quantization of neural networks. , 2017, , .		3
36	A fully pipelined hardware architecture for convolutional neural network with low memory usage and DRAM bandwidth. , 2017, , .		3

#	Article	IF	Citations
37	Adaptive runtime exploiting sparsity in tensor of deep learning neural network on heterogeneous systems. , 2017, , .		7
38	Low-Cost and Steady On-Line Retraining of MLP with Guide Data. Journal of Information Processing, 2017, 25, 820-830.	0.4	0
39	FPGA-based CNN inference accelerator synthesized from multi-threaded C software. , 2017, , .		25
40	Activation-Kernel Extraction through Machine Learning. , 2017, , .		4
41	Technologies for a Thing-Centric Internet of Things. , 2017, , .		3
42	A Comparison between Single Purpose and Flexible Neuromorphic Processor Designs. , 2017, , .		1
43	A method to estimate the energy consumption of deep neural networks. , 2017, , .		90
44	COSY: An Energy-Efficient Hardware Architecture for Deep Convolutional Neural Networks Based on Systolic Array. , 2017, , .		12
45	Conversion of Continuous-Valued Deep Networks to Efficient Event-Driven Networks for Image Classification. Frontiers in Neuroscience, 2017, 11, 682.	2.8	576
46	Sub-uJ deep neural networks for embedded applications. , 2017, , .		1
47	A 200MHZ 202.4GFLOPS@10.8W VGG16 accelerator in Xilinx VX690T. , 2017, , .		12
48	Energy Efficiency Optimizing Based on Characteristics of Machine Learning in Cloud Computing. ITM Web of Conferences, 2017, 12, 03047.	0.5	3
49	IMC. , 2017, , .		8
50	IMCE: Energy-efficient bit-wise in-memory convolution engine for deep neural network. , 2018, , .		38
51	Supporting compressed-sparse activations and weights on SIMD-like accelerator for sparse convolutional neural networks. , 2018, , .		9
52	Exploiting Approximate Feature Extraction via Genetic Programming for Hardware Acceleration in a Heterogeneous Microprocessor. IEEE Journal of Solid-State Circuits, 2018, 53, 1016-1027.	5.4	9
53	An In-Memory VLSI Architecture for Convolutional Neural Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 494-505.	3.6	47
54	Scaling for edge inference of deep neural networks. Nature Electronics, 2018, 1, 216-222.	26.0	299

#	Article	IF	Citations
55	Optimizing the Convolution Operation to Accelerate Deep Neural Networks on FPGA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1354-1367.	3.1	225
56	A Low-Power Circuit for Adaptive Dynamic Programming. , 2018, , .		3
57	Low Cost Convolutional Neural Network Accelerator Based on Bi-Directional Filtering and Bit-Width Reduction. IEEE Access, 2018, 6, 14734-14746.	4.2	11
58	An Architecture to Accelerate Convolution in Deep Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1349-1362.	5.4	80
59	A Multi-Functional In-Memory Inference Processor Using a Standard 6T SRAM Array. IEEE Journal of Solid-State Circuits, 2018, 53, 642-655.	5.4	158
60	Stream Processing Dual-Track CGRA for Object Inference. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1098-1111.	3.1	24
62	Neuromorphic vision chips. Science China Information Sciences, 2018, 61, 1.	4.3	24
63	A 19.4-nJ/Decision, 364-K Decisions/s, In-Memory Random Forest Multi-Class Inference Accelerator. IEEE Journal of Solid-State Circuits, 2018, 53, 2126-2135.	5.4	44
64	Optimizing the data placement and transformation for multi-bank CGRA computing system. , 2018, , .		9
65	Energy-performance design exploration of a low-power microprogrammed deep-learning accelerator. , 2018, , .		4
66	CCR: A concise convolution rule for sparse neural network accelerators. , 2018, , .		7
67	ICNN: An iterative implementation of convolutional neural networks to enable energy and computational complexity aware dynamic approximation. , 2018, , .		27
68	PNeuro: A scalable energy-efficient programmable hardware accelerator for neural networks. , 2018, , .		9
69	MAERI. , 2018, , .		174
70	A Flexible and Energy-Efficient Convolutional Neural Network Acceleration With Dedicated ISA and Accelerator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1408-1412.	3.1	7
71	Recent advances in efficient computation of deep convolutional neural networks. Frontiers of Information Technology and Electronic Engineering, 2018, 19, 64-77.	2.6	178
72	A Scalable Low-Power Reconfigurable Accelerator for Action-Dependent Heuristic Dynamic Programming. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1897-1908.	5.4	3
73	Energy-Efficient Pedestrian Detection System: Exploiting Statistical Error Compensation for Lossy Memory Data Compression. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1301-1311.	3.1	10

#	Article	IF	Citations
74	Parallel Balanced-Bit-Serial Design Technique for Ultra-Low-Voltage Circuits With Energy Saving and Area Efficiency Enhancement. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 141-153.	5.4	3
75	Memristor Crossbar Tiles in a Flexible, General Purpose Neural Processor. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 137-145.	3.6	22
76	Neurostream: Scalable and Energy Efficient Deep Learning with Smart Memory Cubes. IEEE Transactions on Parallel and Distributed Systems, 2018, 29, 420-434.	5.6	61
77	Neuromorphic computing's yesterday, today, and tomorrow â€“ an evolutional view. The Integration VLSI Journal, 2018, 61, 49-61.	2.1	25
78	A 0.55 V 1.1 mW Artificial Intelligence Processor With On-Chip PVT Compensation for Autonomous Mobile Robots. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 567-580.	5.4	8
79	Hardware-Efficient Two-Stage Saliency Detection. , 2018, , .		1
80	To Compress, or Not to Compress: Characterizing Deep Learning Model Compression for Embedded Inference. , 2018, , .		14
81	High-Level Synthesis of Non-Rectangular Multi-Dimensional Nested Loops Using Reshaping and Vectorization. , 2018, , .		0
82	Input-Splitting of Large Neural Networks for Power-Efficient Accelerator with Resistive Crossbar Memory Array. , 2018, , .		17
83	Tolerating Soft Errors in Deep Learning Accelerators with Reliable On-Chip Memory Designs. , 2018, , .		30
84	Multiplication by Inference using Classification Trees: A Case-Study Analysis. , 2018, , .		3
85	Development of Standalone Deep Learning Module for Right Mobile Feature Memory Logic Conjugated System (MLCS). , 2018, , .		0
86	Efficient Deep Convolutional Neural Networks Accelerator without Multiplication and Retraining. , 2018, , .		3
87	Activations Quantization for Compact Neural Networks. , 2018, , .		1
88	A Lightweight Deep Compressive Model for Large-Scale Spike Compression. , 2018, , .		5
89	Mapping Systolic Arrays onto 3D Circuit Structures: Accelerating Convolutional Neural Network Inference. , 2018, , .		12
90	Reducing MAC operation in convolutional neural network with sign prediction. , 2018, , .		10
91	Recurrent Residual Module for Fast Inference in Videos. , 2018, , .		19

#	Article	IF	Citations
92	Accelerator Design for Convolutional Neural Network with Vertical Data Streaming. , 2018, , .		1
93	Energy-Driven Precision Scaling for Fixed-Point ConvNets. , 2018, , .		4
94	Designing adaptive neural networks for energy-constrained image classification. , 2018, , .		40
95	Convolutional Neural Network Accelerator with Reconfigurable Dataflow. , 2018, , .		3
96	A Multi-Mode Accelerator for Pruned Deep Neural Networks. , 2018, , .		0
97	On the Resilience of RTL NN Accelerators: Fault Characterization and Mitigation. , 2018, , .		58
98	Efficient Hardware Realization of Convolutional Neural Networks Using Intra-Kernel Regular Pruning. , 2018, , .		7
99	Cooperative Coevolutionary Approximation in HOG-based Human Detection Embedded System. , 2018, , .		2
100	Towards Memory Friendly Long-Short Term Memory Networks (LSTMs) on Mobile GPUs. , 2018, , .		13
101	Accelerate Convolutional Neural Network with a Customized VLIW DSP. , 2018, , .		0
102	A CGRA based Neural Network Inference Engine for Deep Reinforcement Learning. , 2018, , .		7
103	Diffy: a DÃ©jÃ vu-Free Differential Deep Neural Network Accelerator. , 2018, , .		35
104	Content Addressable Memory Based Binarized Neural Network Accelerator Using Time-Domain Signal Processing. , 2018, , .		2
105	FATE. , 2018, , .		17
106	Approximate Computing Methods for Embedded Machine Learning. , 2018, , .		19
107	Memory Optimization Techniques for FPGA based CNN Implementations. , 2018, , .		10
108	SqueezeNext: Hardware-Aware Neural Network Design. , 2018, , .		179
109	Ultra Power-Efficient CNN Domain Specific Accelerator with 9.3TOPS/Watt for Mobile and Embedded Applications. , 2018, , .		10

#	Article	IF	Citations
110	Mixed-Signal Neuromorphic Inference Accelerators: Recent Results and Future Prospects. , 2018, , .		21
111	Socrates-D 2.0: A Low Power High Throughput Architecture for Deep Network Training. , 2018, , .		0
112	A CNN Accelerator on FPGA Using Depthwise Separable Convolution. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1415-1419.	3.0	130
113	Cambricon-S: Addressing Irregularity in Sparse Neural Networks through A Cooperative Software/Hardware Approach. , 2018, , .		136
114	Design and Implementation of a Neural Network Aided Self-Interference Cancellation Scheme for Full-Duplex Radios. , 2018, , .		29
115	Single-Channel Dataflow for Convolutional Neural Network Accelerator. , 2018, , .		1
116	Edge-Host Partitioning of Deep Neural Networks with Feature Space Encoding for Resource-Constrained Internet-of-Things Platforms. , 2018, , .		95
117	Interpolation-Based Object Detection Using Motion Vectors for Embedded Real-time Tracking Systems. , 2018, , .		15
118	Neuromorphic LIF Row-by-Row Multi-convolution Processor for FPGA. IEEE Transactions on Biomedical Circuits and Systems, 2018, 13, 1-1.	4.0	10
119	A Split-Gate Positive Feedback Device With an Integrate-and-Fire Capability for a High-Density Low-Power Neuron Circuit. Frontiers in Neuroscience, 2018, 12, 704.	2.8	24
120	A Neuromorphic Design Using Chaotic Mott Memristor with Relaxation Oscillation. , 2018, , .		1
121	A High Efficiency Accelerator for Deep Neural Networks. , 2018, , .		1
122	Event-based Row-by-Row Multi-convolution engine for Dynamic-Vision Feature Extraction on FPGA. , 2018, , .		2
123	IONN. , 2018, , .		105
124	AtomLayer: A Universal ReRAM-Based CNN Accelerator with Atomic Layer Computation. , 2018, , .		13
125	DrAcc: a DRAM based Accelerator for Accurate CNN Inference. , 2018, , .		14
126	Minimum Precision Requirements for Deep Learning with Biomedical Datasets. , 2018, , .		2
127	A compression-driven training framework for embedded deep neural networks. , 2018, , .		0

#	Article	IF	Citations
128	An Energy-Efficient and Flexible Accelerator based on Reconfigurable Computing for Multiple Deep Convolutional Neural Networks. , 2018, , .		6
129	Multi-dimensional Parallel Training of Winograd Layer on Memory-Centric Architecture. , 2018, , .		10
130	Comprehensive Evaluation of Supply Voltage Underscaling in FPGA on-Chip Memories. , 2018, , .		32
131	Design Tradeoff of Internal Memory Size and Memory Access Energy in Deep Neural Network Hardware Accelerators. , 2018, , .		3
132	Study on the Optimization of CNN Based on Image Identification. , 2018, , .		6
133	A Computing Efficient Hardware Architecture for Sparse Deep Neural Network Computing. , 2018, , .		1
134	An Asynchronous Energy-Efficient CNN Accelerator with Reconfigurable Architecture. , 2018, , .		7
135	Role Assignment in IoT Through Accelerated Hardware. , 2018, , .		1
136	Benchmarking and Analyzing Deep Neural Network Training. , 2018, , .		82
137	Cross-layer efforts for energy-efficient computing: towards peta operations per second per watt. Frontiers of Information Technology and Electronic Engineering, 2018, 19, 1209-1223.	2.6	5
138	LerGAN: A Zero-Free, Low Data Movement and PIM-Based GAN Architecture. , 2018, , .		22
139	An Analytical Method to Determine Minimum Per-Layer Precision of Deep Neural Networks. , 2018, , .		22
140	An Unsupervised Anomalous Event Detection Framework with Class Aware Source Separation. , 2018, , .		6
141	Hardware-aware machine learning. , 2018, , .		27
142	Energy-Efficient Speaker Identification with Low-Precision Networks. , 2018, , .		2
143	Perspective: Uniform switching of artificial synapses for large-scale neuromorphic arrays. APL Materials, 2018, 6, .	5.1	26
144	Eadnet: Efficient Architecture for Decomposed Convolutional Neural Networks. , 2018, , .		0
145	SNrram: An Efficient Sparse Neural Network Computation Architecture Based on Resistive Random-Access Memory. , 2018, , .		32

#	Article	IF	Citations
146	TRIG: Hardware Accelerator for Inference-Based Applications and Experimental Demonstration Using Carbon Nanotube FETs. , 2018, , .		3
147	DPS: Dynamic Precision Scaling for Stochastic Computing-based Deep Neural Networks. , 2018, , .		13
148	DyHard-DNN: Even More DNN Acceleration with Dynamic Hardware Reconfiguration. , 2018, , .		1
149	An Intelligent Bandwidth Manager for CNN Applications on Embedded Devices. , 2018, , .		0
150	iFPNA: A Flexible and Efficient Deep Neural Network Accelerator with a Programmable Data Flow Engine in 28nm CMOS. , 2018, , .		6
151	CoNNA â€“ Compressed CNN Hardware Accelerator. , 2018, , .		14
152	True Gradient-Based Training of Deep Binary Activated Neural Networks Via Continuous Binarization. , 2018, , .		12
153	Deep compressive autoencoder for action potential compression in large-scale neural recording. Journal of Neural Engineering, 2018, 15, 066019.	3.5	34
154	Mosaic-CNN: A Combined Two-Step Zero Prediction Approach to Trade off Accuracy and Computation Energy in Convolutional Neural Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 770-781.	3.6	16
155	Atomlayer. , 2018, , .		63
156	Exploring the Programmability for Deep Learning Processors: from Architecture to Tensorization. , 2018, , .		0
157	Dyhard-DNN. , 2018, , .		16
158	A Variation-Tolerant In-Memory Machine Learning Classifier via On-Chip Training. IEEE Journal of Solid-State Circuits, 2018, 53, 3163-3173.	5.4	89
159	Automatic Modulation Classification: A Deep Learning Enabled Approach. IEEE Transactions on Vehicular Technology, 2018, 67, 10760-10772.	6.3	227
160	A 2.56-mm² 718GOPS Configurable Spiking Convolutional Sparse Coding Accelerator in 40-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 2818-2827.	5.4	3
161	Approximate Fully Connected Neural Network Generation. , 2018, , .		4
162	A 141.4 mW Low-Power Online Deep Neural Network Training Processor for Real-time Object Tracking in Mobile Devices. , 2018, , .		11
163	A writeâ€improved lowâ€power 12T SRAM cell for wearable wireless sensor nodes. International Journal of Circuit Theory and Applications, 2018, 46, 2314-2333.	2.0	39

#	Article	IF	Citations
164	Advanced Topics in Deep Learning. , 2018, , 419-458.		0
165	Design Space Exploration for Orlando Ultra Low-Power Convolutional Neural Network SoC. , 2018, , .		6
166	Configurable CNN Accelerator Based on Tiling Dataflow. , 2018, , .		2
167	Opportunities for Machine Learning in Electronic Design Automation. , 2018, , .		20
168	Hardware for machine learning: Challenges and opportunities. , 2018, , .		35
169	Implementation of a CNN accelerator on an Embedded SoC Platform using SDSoC. , 2018, , .		5
170	Sparseness Ratio Allocation and Neuron Re-pruning for Neural Networks Compression. , 2018, , .		0
171	Content addressable memory based binarized neural network accelerator using time-domain signal processing. , 2018, , .		7
172	DPS. , 2018, , .		21
173	A neuromorphic design using chaotic mott memristor with relaxation oscillation. , 2018, , .		0
174	Lossy Compression for Embedded Computer Vision Systems. IEEE Access, 2018, 6, 39385-39397.	4.2	16
175	Big-BOE: Fusing Spanish Official Gazette with Big Data Technology. Big Data, 2018, 6, 124-138.	3.4	9
176	ASIC Implementation of a Nonlinear Dynamical Model for Hippocampal Prosthesis. Neural Computation, 2018, 30, 2472-2499.	2.2	2
177	Structured Weight Matrices-Based Hardware Accelerators in Deep Neural Networks. , 2018, , .		17
178	Compact Convolution Mapping on Neuromorphic Hardware using Axonal Delay. , 2018, , .		1
179	Quasi-exact logic functions through classification trees. The Integration VLSI Journal, 2018, 63, 248-255.	2.1	2
180	GANAX: A Unified MIMD-SIMD Acceleration for Generative Adversarial Networks. , 2018, , .		58
181	Biomedical Image Segmentation Using Fully Convolutional Networks on TrueNorth. , 2018, , .		3

#	Article	IF	Citations
182	Euphrates: Algorithm-SoC Co-Design for Low-Power Mobile Continuous Vision. , 2018, , .		51
183	Bit Fusion: Bit-Level Dynamically Composable Architecture for Accelerating Deep Neural Network. , 2018, , .		284
184	Design and Application Space Exploration of a Domain-Specific Accelerator System. Electronics (Switzerland), 2018, 7, 45.	3.1	3
185	Relative indexed compressed sparse filter encoding format for hardware-oriented acceleration of deep convolutional neural networks. , 2018, , .		0
186	GNA: Reconfigurable and Efficient Architecture for Generative Network Acceleration. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2519-2529.	2.7	35
187	PAGURUS: Low-Overhead Dynamic Information Flow Tracking on Loosely Coupled Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2685-2696.	2.7	16
188	Mapping of local and global synapses on spiking neuromorphic hardware. , 2018, , .		40
189	Maximizing system performance by balancing computation loads in LSTM accelerators. , 2018, , .		15
190	A 3D Tiled Low Power Accelerator for Convolutional Neural Network. , 2018, , .		9
191	Neuro-NoC: Energy Optimization in Heterogeneous Many-Core NoC using Neural Networks in Dark Silicon Era. , 2018, , .		13
192	Artificial intelligence meets large-scale sensing: Using Large-Area Electronics (LAE) to enable intelligent spaces. , 2018, , .		8
193	Google Workloads for Consumer Devices. , 2018, , .		134
194	Optimally Removing Synchronization Overhead for CNNs in Three-Dimensional Neuromorphic Architecture. IEEE Transactions on Industrial Electronics, 2018, 65, 8973-8981.	7.9	4
195	A Convolutional Accelerator for Neural Networks With Binary Weights. , 2018, , .		11
196	Artificial Intelligence: The Future Landscape of Genomic Medical Diagnosis: Dataset, In Silico Artificial Intelligent Clinical Information, and Machine Learning Systems. , 2018, , 223-267.		1
197	EVAÂ²: Exploiting Temporal Redundancy in Live Computer Vision. , 2018, , .		44
198	Achieving Low Power Classification with Classifier Ensemble. , 2018, , .		1
199	Dynamic Bit-width Reconfiguration for Energy-Efficient Deep Learning Hardware. , 2018, , .		17

#	Article	IF	Citations
200	Accelerating Low Bit-Width Deep Convolution Neural Network in MRAM. , 2018, , .		13
201	An FPGA Implementation of a Convolutional Auto-Encoder. Applied Sciences (Switzerland), 2018, 8, 504.	2.5	10
202	Improving Deep Learning with a customizable GPU-like FPGA-based accelerator. , 2018, , .		1
203	Hardware Implementation of Reconfigurable Separable Convolution. , 2018, , .		1
204	Streaming Tiles: Flexible Implementation of Convolution Neural Networks Inference on Manycore Architectures. , 2018, , .		0
205	An Optimized Architecture For Decomposed Convolutional Neural Networks. , 2018, , .		0
206	VIBNN. , 2018, , .		39
207	Deep Learning for IoT Big Data and Streaming Analytics: A Survey. IEEE Communications Surveys and Tutorials, 2018, 20, 2923-2960.	39.4	905
208	Recent progress in analog memory-based accelerators for deep learning. Journal Physics D: Applied Physics, 2018, 51, 283001.	2.8	173
209	Energy-Efficient Convolution Architecture Based on Rescheduled Dataflow. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4196-4207.	5.4	45
210	Analyzing and mitigating the impact of permanent faults on a systolic array based neural network accelerator. , 2018, , .		101
211	An Energy Efficient JPEG Encoder with Neural Network Based Approximation and Near-Threshold Computing. , 2018, , .		2
212	SmartShuttle: Optimizing off-chip memory accesses for deep learning accelerators. , 2018, , .		66
213	Implementation of multilayer perceptron network with highly uniform passive memristive crossbar circuits. Nature Communications, 2018, 9, 2331.	12.8	281
214	Generalized Water-filling for Source-aware Energy-efficient SRAMs. IEEE Transactions on Communications, 2018, , 1-1.	7.8	12
215	Design Exploration of IoT centric Neural Inference Accelerators. , 2018, , .		7
216	Design-Space Exploration of Pareto-Optimal Architectures for Deep Learning with DVFS. , 2018, , .		5
217	In-memory computing with resistive switching devices. Nature Electronics, 2018, 1, 333-343.	26.0	1,316

#	Article	IF	Citations
218	A Multi-Mode Visual Recognition Hardware Accelerator for AR/MR Glasses. , 2018, , .		1
219	Sustainable CNN for Robotic: An Offloading Game in the 3D Vision Computation. IEEE Transactions on Sustainable Computing, 2019, 4, 67-76.	3.1	11
220	FPAP: A Folded Architecture for Energy-Quality Scalable Convolutional Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 288-301.	5.4	10
221	SensorNet: A Scalable and Low-Power Deep Convolutional Neural Network for Multimodal Data Classification. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 274-287.	5.4	62
222	A Real-Time Convolutional Neural Network for Super-Resolution on FPGA With Applications to 4K UHD 60 fps Video Services. IEEE Transactions on Circuits and Systems for Video Technology, 2019, 29, 2521-2534.	8.3	59
223	Addressing Sparsity in Deep Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1858-1871.	2.7	10
224	Hierarchical Memory System With STT-MRAM and SRAM to Support Transfer and Real-Time Reinforcement Learning in Autonomous Drones. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 485-497.	3.6	13
225	WRA: A 2.2-to-6.3 TOPS Highly Unified Dynamically Reconfigurable Accelerator Using a Novel Winograd Decomposition Algorithm for Convolutional Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3480-3493.	5.4	23
226	Using Frame Similarity for Low Energy Software-Only IoT Video Recognition. Lecture Notes in Computer Science, 2019, , 157-168.	1.3	0
227	Tightly Coupled Machine Learning Coprocessor Architecture With Analog In-Memory Computing for Instruction-Level Acceleration. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 544-561.	3.6	4
228	DeLTA: GPU Performance Model for Deep Learning Applications with In-Depth Memory System Traffic Analysis. , 2019, , .		24
229	Hardware implementation of RRAM based binarized neural networks. APL Materials, 2019, 7, .	5.1	16
230	An Energy-Efficient Accelerator with Relative- Indexing Memory for Sparse Compressed Convolutional Neural Network. , 2019, , .		3
231	Dual-Precision Acceleration of Convolutional Neural Network Computation with Mixed Input and Output Data Reuse. , 2019, , .		1
232	An 8 Bit 12.4 TOPS/W Phase-Domain MAC Circuit for Energy-Constrained Deep Learning Accelerators. IEEE Journal of Solid-State Circuits, 2019, 54, 2730-2742.	5.4	17
233	Analog Neural Networks With Deep-Submicrometer Nonlinear Synapses. IEEE Micro, 2019, 39, 55-63.	1.8	3
234	A Multilayer-Learning Current-Mode Neuromorphic System With Analog-Error Compensation. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 986-998.	4.0	4
235	Heterogeneous Activation Function Extraction for Training and Optimization of SNN Systems. , 2019, , .		0

#	Article	IF	Citations
236	A High Efficient Architecture for Convolution Neural Network Accelerator. , 2019, , .		2
237	EdgeL^3: Compressing L^3-Net for Mote Scale Urban Noise Monitoring. , 2019, , .		6
238	Leveraging Independent Double-Gate FinFET Devices for Machine Learning Classification. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4356-4367.	5.4	10
239	Distributed Communicating Neural Network Architecture for Smart Environments. , 2019, , .		2
240	Energy-Efficient Inference Accelerator for Memory-Augmented Neural Networks on an FPGA. , 2019, , .		4
241	A 2.17mW Acoustic DSP Processor with CNN-FFT Accelerators for Intelligent Hearing Aided Devices. , 2019, , .		3
242	Benchmark of Ferroelectric Transistor-Based Hybrid Precision Synapse for Neural Network Accelerator. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 142-150.	1.5	20
243	Sensitivity-Based Error Resilient Techniques With Heterogeneous Multiplyâ€“Accumulate Unit for Voltage Scalable Deep Neural Network Accelerators. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 520-531.	3.6	16
244	Intelligent Computing with RRAM. , 2019, , .		2
245	Methodology for Efficient Reconfigurable Architecture of Generative Neural Network. , 2019, , .		7
246	Supporting peripherals in intermittent systems with just-in-time checkpoints. , 2019, , .		59
247	Guaranteed Compression Rate for Activations in CNNs using a Frequency Pruning Approach. , 2019, , .		1
248	Eager pruning. , 2019, , .		42
249	A Resources-Efficient Configurable Accelerator for Deep Convolutional Neural Networks. IEEE Access, 2019, 7, 72113-72124.	4.2	21
250	Convolutional Neural Network Accelerator with Vector Quantization. , 2019, , .		2
251	mRNA: Enabling Efficient Mapping Space Exploration for a Reconfiguration Neural Accelerator. , 2019, , .		22
252	NNSim: A Fast and Accurate SystemC/TLM Simulator for Deep Convolutional Neural Network Accelerators. , 2019, , .		3
253	Efficient Dynamic Fixed-Point Quantization of CNN Inference Accelerators for Edge Devices. , 2019, , .		8

#	Article	IF	Citations
254	Learn-to-Scale: Parallelizing Deep Learning Inference on Chip Multiprocessor Architecture. , 2019, , .		7
255	Sparse ReRAM engine. , 2019, , .		121
256	Low-Complexity Dynamic Channel Scaling of Noise-Resilient CNN for Intelligent Edge Devices. , 2019, , .		6
257	Hardware Efficient Convolution Processing Unit for Deep Neural Networks. , 2019, , .		3
258	On-device facial verification using NUF-Net model of deep learning. Engineering Applications of Artificial Intelligence, 2019, 85, 579-589.	8.1	9
259	Towards artificial general intelligence with hybrid Tianjic chip architecture. Nature, 2019, 572, 106-111.	27.8	517
260	PIR-DSP: An FPGA DSP Block Architecture for Multi-precision Deep Neural Networks. , 2019, , .		28
261	Efficient Modular Adder Designs Based on Thermometer and One-Hot Coding. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2142-2155.	3.1	20
262	iFPNA: A Flexible and Efficient Deep Learning Processor in 28-nm CMOS Using a Domain-Specific Instruction Set and Reconfigurable Fabric. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 346-357.	3.6	5
263	Custom Sub-Systems and Circuits for Deep Learning: Guest Editorial Overview. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 247-252.	3.6	2
264	Understanding Reuse, Performance, and Hardware Cost of DNN Dataflow. , 2019, , .		151
265	eCNN. , 2019, , .		37
266	Manna. , 2019, , .		15
267	Cost Forecasting Model of Transformer Substation Projects Based on Data Inconsistency Rate and Modified Deep Convolutional Neural Network. Energies, 2019, 12, 3043.	3.1	2
268	Sparse Tensor Core. , 2019, , .		65
269	Design Methodology for Embedded Approximate Artificial Neural Networks. , 2019, , .		9
270	Aggressive Energy Reduction for Video Inference with Software-only Strategies. Transactions on Embedded Computing Systems, 2019, 18, 1-20.	2.9	3
271	A Software-Hardware collaboration system for CNN algorithms based on FPGA. , 2019, , .		0

#	Article	IF	Citations
272	Spatial Data Dependence Graph Simulator for Convolutional Neural Network Accelerators. , 2019, , .		2
273	An Accelerator-based Architecture Utilizing an Efficient Memory Link for Modern Computational Requirements. , 2019, , .		2
274	DNN pruning and mapping on NoC-Based communication infrastructure. Microelectronics Journal, 2019, 94, 104655.	2.0	16
275	NoC-based DNN accelerator. , 2019, , .		37
277	dMazeRunner. Transactions on Embedded Computing Systems, 2019, 18, 1-27.	2.9	48
278	ReBNN: in-situ acceleration of binarized neural networks in ReRAM using complementary resistive cell. CCF Transactions on High Performance Computing, 2019, 1, 196-208.	1.7	11
279	On-Chip Instruction Generation for Cross-Layer CNN Accelerator on FPGA. , 2019, , .		4
280	CompAct. Transactions on Embedded Computing Systems, 2019, 18, 1-24.	2.9	13
281	Direct Feedback Alignment With Sparse Connections for Local Learning. Frontiers in Neuroscience, 2019, 13, 525.	2.8	28
282	Accelerating CNN-RNN Based Machine Health Monitoring on FPGA. , 2019, , .		3
283	Acceleration of DNN Backward Propagation by Selective Computation of Gradients. , 2019, , .		9
284	An Application-Specific VLIW Processor with Vector Instruction Set for CNN Acceleration. , 2019, , .		6
285	Impact of Non-Ideal Characteristics of Resistive Synaptic Devices on Implementing Convolutional Neural Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 570-579.	3.6	100
286	Hardware Complexity Analysis of Deep Neural Networks and Decision Tree Ensembles for Real-time Neural Data Classification. , 2019, , .		18
287	A Perspective on Test Methodologies for Supervised Machine Learning Accelerators. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 562-569.	3.6	9
288	Edge and Fog Computing Enabled AI for IoT-An Overview. , 2019, , .		40
289	Incremental Learning Meets Reduced Precision Networks. , 2019, , .		2
290	Transfer and Online Reinforcement Learning in STT-MRAM Based Embedded Systems for Autonomous Drones. , 2019, , .		7

#	Article	IF	Citations
291	Estimation of energy consumption in machine learning. Journal of Parallel and Distributed Computing, 2019, 134, 75-88.	4.1	254
292	Special Session: 2018 Low-Power Image Recognition Challenge and Beyond. , 2019, , .		0
293	Accelerator Design for Vector Quantized Convolutional Neural Network. , 2019, , .		2
294	USCA: A Unified Systolic Convolution Array Architecture for Accelerating Sparse Neural Network. , 2019, , .		10
295	Neural Models of Ferrite Inductors Non-Linear Behavior. , 2019, , .		10
296	Systolic Building Block for Logic-on-Logic 3D-IC Implementations of Convolutional Neural Networks. , 2019, , .		5
297	A Flexible and High-Performance Self-Organizing Feature Map Training Acceleration Circuit and Its Applications. , 2019, , .		3
298	Smilodon: An Efficient Accelerator for Low Bit-Width CNNs with Task Partitioning. , 2019, , .		4
299	YOLO-Based Valve Type Recognition and Localization. , 2019, , .		5
300	Efficient Network Construction Through Structural Plasticity. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 453-464.	3.6	8
301	A Historical Perspective on Hardware AI Inference, Charge-Based Computational Circuits and an 8 bit Charge-Based Multiply-Add Core in 16 nm FinFET CMOS. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 532-543.	3.6	11
302	Multi-level Weight Indexing Scheme for Memory-Reduced Convolutional Neural Network. , 2019, , .		3
303	DeepTools: Compiler and Execution Runtime Extensions for RaPiD AI Accelerator. IEEE Micro, 2019, 39, 102-111.	1.8	14
304	A stochastic-computing based deep learning framework using adiabatic quantum-flux-parametron superconducting technology. , 2019, , .		27
305	Data Locality Optimization of Depthwise Separable Convolutions for CNN Inference Accelerators. , 2019, , .		5
306	Towards Cross-Platform Inference on Edge Devices with Emerging Neuromorphic Architecture. , 2019, , .		3
307	A Survey of Convolutional Neural Networks on Edge with Reconfigurable Computing. Algorithms, 2019, 12, 154.	2.1	75
308	In situ training of feed-forward and recurrent convolutional memristor networks. Nature Machine Intelligence, 2019, 1, 434-442.	16.0	201

#	Article	IF	Citations
309	An efficient ReRAM-based inference accelerator for convolutional neural networks via activation reuse. IEICE Electronics Express, 2019, 16, 20190396-20190396.	0.8	4
310	A 1.8mW Perception Chip with Near-Sensor Processing Scheme for Low-Power AIoT Applications. , 2019, , .		3
311	A Logic Compatible 4T Dual Embedded DRAM Array for In-Memory Computation of Deep Neural Networks. , 2019, , .		17
312	An Energy-Aware Bit-Serial Streaming Deep Convolutional Neural Network Accelerator. , 2019, , .		0
313	An Adaptive Memory Management Strategy Towards Energy Efficient Machine Inference in Event-Driven Neuromorphic Accelerators. , 2019, , .		1
314	Edge Intelligence based Co-training of CNN. , 2019, , .		5
315	Design of A Bit-Serial Artificial Neuron VLSI Architecture with Early Termination. , 2019, , .		0
317	A Power and Area Efficient CMOS Stochastic Neuron for Neural Networks Employing Resistive Crossbar Array. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 1678-1689.	4.0	7
318	An Efficient Streaming Accelerator for Low Bit-Width Convolutional Neural Networks. Electronics (Switzerland), 2019, 8, 371.	3.1	4
319	Cell division. , 2019, , .		1
320	FLightNNs. , 2019, , .		14
321	Customized High Performance and Energy Efficient Communication Networks for AI Chips. IEEE Access, 2019, 7, 69434-69446.	4.2	10
322	Energy-Accuracy Scalable Deep Convolutional Neural Networks: A Pareto Analysis. IFIP Advances in Information and Communication Technology, 2019, , 107-127.	0.7	1
323	A Primer on Deep Learning Architectures and Applications in Speech Processing. Circuits, Systems, and Signal Processing, 2019, 38, 3406-3432.	2.0	16
324	XNOR-SRAM. , 2019, , .		9
325	Xcel-RAM: Accelerating Binary Neural Networks in High-Throughput SRAM Compute Arrays. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3064-3076.	5.4	65
326	SeFAct. , 2019, , .		5
327	Deep Neural Network Approximation for Custom Hardware. ACM Computing Surveys, 2020, 52, 1-39.	23.0	88

#	Article	IF	Citations
328	A Heterogeneous and Reconfigurable Embedded Architecture for Energy-Efficient Execution of Convolutional Neural Networks. Lecture Notes in Computer Science, 2019, , 267-280.	1.3	4
329	HSIM-DNN. , 2019, , .		3
330	An In-DRAM Neural Network Processing Engine. , 2019, , .		10
331	TANGRAM. , 2019, , .		80
332	Pre-Defined Sparse Neural Networks With Hardware Acceleration. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 332-345.	3.6	11
333	Systolic Cube. , 2019, , .		12
334	DT-CNN: Dilated and Transposed Convolution Neural Network Accelerator for Real-Time Image Segmentation on Mobile Devices. , 2019, , .		26
335	VIP: A Versatile Inference Processor. , 2019, , .		5
336	Optimizing Weight Mapping and Data Flow for Convolutional Neural Networks on RRAM Based Processing-In-Memory Architecture. , 2019, , .		55
337	A Low-latency Sparse-Winograd Accelerator for Convolutional Neural Networks. , 2019, , .		20
338	High-Performance FPGA-Based CNN Accelerator With Block-Floating-Point Arithmetic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1874-1885.	3.1	100
339	InsideNet: A tool for characterizing convolutional neural networks. Future Generation Computer Systems, 2019, 100, 298-315.	7.5	3
340	Towards the Development of Analog Neuromorphic Chip Prototype with 2.4M Integrated Memristors. , 2019, , .		10
341	Data-Retention-Time Characterization of Gain-Cell eDRAMs Across the Design and Variations Space. , 2019, , .		2
342	An MRAM-Based Deep In-Memory Architecture for Deep Neural Networks. , 2019, , .		28
343	A Binarized Neural Network Accelerator with Differential Crosspoint Memristor Array for Energy-Efficient MAC Operations. , 2019, , .		11
344	Hardware Trojan Design on Neural Networks. , 2019, , .		40
345	Large-Scale Optical Neural Networks Based on Photoelectric Multiplication. Physical Review X, 2019, 9, .	8.9	179

#	Article	IF	Citations
346	Compact Convolutional Neural Network Accelerator for IoT Endpoint SoC. Electronics (Switzerland), 2019, 8, 497.	3.1	13
347	Packing Sparse Convolutional Neural Networks for Efficient Systolic Array Implementations. , 2019, , .		94
348	Eyeriss v2: A Flexible Accelerator for Emerging Deep Neural Networks on Mobile Devices. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 292-308.	3.6	609
349	HyPar: Towards Hybrid Parallelism for Deep Learning Accelerator Array. , 2019, , .		64
350	Bit Prudent In-Cache Acceleration of Deep Convolutional Neural Networks. , 2019, , .		24
351	Shortcut Mining: Exploiting Cross-Layer Shortcut Reuse in DCNN Accelerators. , 2019, , .		30
352	NAND-Net: Minimizing Computational Complexity of In-Memory Processing for Binary Neural Networks. , 2019, , .		25
353	Small Memory Footprint Neural Network Accelerators. , 2019, , .		6
354	14.1 A 65nm 1.1-to-9.1TOPS/W Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Model-Based and Model-Free Swarm Robotics. , 2019, , .		12
355	NeuralHMC. , 2019, , .		9
356	DeepRT: predictable deep learning inference for cyber-physical systems. Real-Time Systems, 2019, 55, 106-135.	1.3	10
357	Compute-Efficient Neural-Network Acceleration. , 2019, , .		14
358	A 64-Tile 2.4-Mb In-Memory-Computing CNN Accelerator Employing Charge-Domain Compute. IEEE Journal of Solid-State Circuits, 2019, 54, 1789-1799.	5.4	182
359	Deep Learning-Based Multiple Object Visual Tracking on Embedded System for IoT and Mobile Edge Computing Applications. IEEE Internet of Things Journal, 2019, 6, 5423-5431.	8.7	70
360	Adaptive Quantization as a Device-Algorithm Co-Design Approach to Improve the Performance of In-Memory Unsupervised Learning With SNNs. IEEE Transactions on Electron Devices, 2019, 66, 1722-1728.	3.0	8
361	NNBench-X: Benchmarking and Understanding Neural Network Workloads for Accelerator Designs. IEEE Computer Architecture Letters, 2019, 18, 38-42.	1.5	6
362	An N-way group association architecture and sparse data group association load balancing algorithm for sparse CNN accelerators. , 2019, , .		10
363	Parallelism-flexible Convolution Core for Sparse Convolutional Neural Networks on FPGA. IPSJ Transactions on System LSI Design Methodology, 2019, 12, 22-37.	0.8	3

#	Article	IF	Citations
364	Optimize Deep Convolutional Neural Network with Ternarized Weights and High Accuracy. , 2019, , .		12
365	REQ-YOLO. , 2019, , .		67
366	1.1 Deep Learning Hardware: Past, Present, and Future. , 2019, , .		91
367	Machine Learning With Neuromorphic Photonics. Journal of Lightwave Technology, 2019, 37, 1515-1534.	4.6	129
368	A State-of-the-Art Survey on Deep Learning Theory and Architectures. Electronics (Switzerland), 2019, 8, 292.	3.1	954
369	Reinforcement learning with analogue memristor arrays. Nature Electronics, 2019, 2, 115-124.	26.0	247
370	Breaking High-Resolution CNN Bandwidth Barriers With Enhanced Depth-First Execution. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 323-331.	3.6	33
371	Deep Learning-Based Channel Estimation for Doubly Selective Fading Channels. IEEE Access, 2019, 7, 36579-36589.	4.2	173
372	Artificial intelligence to diagnose meniscus tears on MRI. Diagnostic and Interventional Imaging, 2019, 100, 243-249.	3.2	65
373	A High-Throughput and Power-Efficient FPGA Implementation of YOLO CNN for Object Detection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1861-1873.	3.1	292
374	Orbital Edge Computing: Machine Inference in Space. IEEE Computer Architecture Letters, 2019, 18, 59-62.	1.5	47
375	ReRAM-Based In-Memory Computing for Search Engine and Neural Network Applications. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 388-397.	3.6	33
376	How to Measure Energy Consumption in Machine Learning Algorithms. Lecture Notes in Computer Science, 2019, , 243-255.	1.3	7
377	Deep Learning for Electromyographic Hand Gesture Signal Classification Using Transfer Learning. IEEE Transactions on Neural Systems and Rehabilitation Engineering, 2019, 27, 760-771.	4.9	440
378	A 1920 $imes$ 1080 25-Frames/s 2.4-TOPS/W Low-Power 6-D Vision Processor for Unified Optical Flow and Stereo Depth With Semi-Global Matching. IEEE Journal of Solid-State Circuits, 2019, 54, 1048-1058.	5.4	20
379	The Evaluation of DCNN on Vector-SIMD DSP. IEEE Access, 2019, 7, 22301-22309.	4.2	10
380	A 290-mV, 7-nm Ultra-Low-Voltage One-Port SRAM Compiler Design Using a 12T Write Contention and Read Upset Free Bit-Cell. IEEE Journal of Solid-State Circuits, 2019, 54, 1152-1160.	5.4	9
381	A Real-Time and Hardware-Efficient Processor for Skeleton-Based Action Recognition With Lightweight Convolutional Neural Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 2052-2056.	3.0	13

#	Article	IF	Citations
382	Efficient FPGA implementation of local binary convolutional neural network. , 2019, , .		3
383	ECML PKDD 2018 Workshops. Lecture Notes in Computer Science, 2019, , .	1.3	2
384	Design of multicycle path accelerator for neural network. , 2019, , .		0
385	Fast Simulation Method for Analog Deep Binarized Neural Networks. , 2019, , .		1
386	Condensation-Net: Memory-Efficient Network Architecture With Cross-Channel Pooling Layers and Virtual Feature Maps. , 2019, , .		3
387	DHP19: Dynamic Vision Sensor 3D Human Pose Dataset. , 2019, , .		36
388	The Implementation of LeNet-5 with NVDLA on RISC-V SoC. , 2019, , .		6
389	DASNet: Dynamic Activation Sparsity for Neural Network Efficiency Improvement. , 2019, , .		7
390	TapirXLA: Embedding Fork-Join Parallelism into the XLA Compiler in TensorFlow Using Tapir. , 2019, , .		2
391	AX-DBN: An Approximate Computing Framework for the Design of Low-Power Discriminative Deep Belief Networks. , 2019, , .		1
392	Understanding the Impact of On-chip Communication on DNN Accelerator Performance. , 2019, , .		11
393	DynExit: A Dynamic Early-Exit Strategy for Deep Residual Networks. , 2019, , .		15
394	Accelergy: An Architecture-Level Energy Estimation Methodology for Accelerator Designs. , 2019, , .		113
395	LHC: A Low-Power Heterogeneous Computing Method on Neural Network Accelerator. , 2019, , .		0
396	A Configurable and Versatile Architecture for Low Power, Energy Efficient Hardware Acceleration of Convolutional Neural Networks. , 2019, , .		0
397	Design of Low Power Multiplier for Vision chips. , 2019, , .		0
398	NR-MPA: Non-Recovery Compression Based Multi-Path Packet-Connected-Circuit Architecture of Convolution Neural Networks Accelerator. , 2019, , .		1
399	High Throughput Hardware Implementation for Deep Learning AI Accelerator. , 2019, , .		1

#	Article	IF	Citations
400	Power Analysis Resilient SRAM Design Implemented with a 1% Area Overhead Impedance Randomization Unit for Security Applications. , 2019, , .		3
401	Data Optimization CNN Accelerator Design on FPGA. , 2019, , .		8
402	Automatic Hardware Design Tool Based on Reusing Transformation. , 2019, , .		2
403	PyRTLMatrix: An Object-Oriented Hardware Design Pattern for Prototyping ML Accelerators. , 2019, , .		1
404	An Energy-Efficient In-Memory BNN Architecture With Time-Domain Analog and Digital Mixed-Signal Processing. , 2019, , .		2
405	DupNet: Towards Very Tiny Quantized CNN With Improved Accuracy for Face Detection. , 2019, , .		2
406	Customizing CMOS/ReRAM Hybrid Hardware Architecture for Spiking CNN. , 2019, , .		0
407	Data-Driven Neuromorphic DRAM-based CNN and RNN Accelerators. , 2019, , .		3
408	Optimal Input-Dependent Edge-Cloud Partitioning for RNN Inference. , 2019, , .		2
409	Neuromorphic Hardware Accelerator for SNN Inference based on STT-RAM Crossbar Arrays. , 2019, , .		9
410	GenUnlock: An Automated Genetic Algorithm Framework for Unlocking Logic Encryption. , 2019, , .		16
411	A Zero-Gating Processing Element Design for Low-Power Deep Convolutional Neural Networks. , 2019, , .		3
412	FPGA Based Implementations of RNN and CNN: A Brief Analysis. , 2019, , .		42
413	MoNA: Mobile Neural Architecture with Reconfigurable Parallel Dimensions. , 2019, , .		1
414	A Quantized Neural Network Library for Proper Implementation of Hardware Emulation. , 2019, , .		3
415	Characterizing the Deployment of Deep Neural Networks on Commercial Edge Devices. , 2019, , .		58
416	Latency-Insensitive Controller for Convolutional Neural Network Accelerators. , 2019, , .		2
417	Outlier-aware Time-multiplexing MAC for Higher Energy-Efficiency on CNNs. , 2019, , .		0

#	Article	IF	Citations
418	Flexible Low Power CNN Accelerator for Edge Computing with Weight Tuning. , 2019, , .		4
419	Dynamic Thermal-Aware Inter-Layer Perpendicular Downward Mapping for Three-Dimensional Convolutional Neural Network Accelerator. , 2019, , .		0
420	Design of a DBN Hardware Accelerator for Handwritten Digit Recognitions. , 2019, , .		1
421	Vesti: An In-Memory Computing Processor for Deep Neural Networks Acceleration. , 2019, , .		1
422	Performance-driven Programming of Multi-TFLOP Deep Learning Accelerators*. , 2019, , .		1
423	Benchmarking Contemporary Deep Learning Hardware and Frameworks: A Survey of Qualitative Metrics. , 2019, , .		23
424	Evaluation of a Chained Systolic Array with High-Speed Links. , 2019, , .		1
425	Conversion of Artificial Neural Network to Spiking Neural Network for Hardware Implementation. , 2019, , .		1
426	A Low-Power High-Throughput In-Memory CMOS-ReRAM Accelerator for Large-Scale Deep Residual Neural Networks. , 2019, , .		1
427	Exploring Resource-Efficient Acceleration Algorithm for Transposed Convolution of GANs on FPGA. , 2019, , .		5
428	A Hardware Inference Accelerator for Temporal Convolutional Networks. , 2019, , .		1
429	Adaptive Filtering in In-Memory-Based Architectures. , 2019, , .		1
430	Direct Feedback Alignment Based Convolutional Neural Network Training for Low-Power Online Learning Processor. , 2019, , .		4
431	A Low-Power Spike-Like Neural Network Design. Electronics (Switzerland), 2019, 8, 1479.	3.1	6
432	A Block-Floating-Point Arithmetic Based FPGA Accelerator for Convolutional Neural Networks. , 2019, , .		1
433	A RISC-V based hardware accelerator designed for Yolo object detection system. , 2019, , .		17
434	An Efficient Event-driven Neuromorphic Architecture for Deep Spiking Neural Networks. , 2019, , .		2
435	A Power-Efficient Programmable DCNN Processor for Intelligent Sensing. , 2019, , .		0

#	Article	IF	Citations
436	ReCoN: A Reconfigurable CNN Acceleration Framework for Hybrid Semantic Segmentation on Hybrid SoCs for Space Applications. , 2019, , .		7
437	Review and Benchmarking of Precision-Scalable Multiply-Accumulate Unit Architectures for Embedded Neural-Network Processing. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 697-711.	3.6	50
438	Retrain-Less Weight Quantization for Multiplier-Less Convolutional Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 972-982.	5.4	13
439	A streaming accelerator of Convolutional Neural Networks for resource-limited applications. IEICE Electronics Express, 2019, 16, 20190633-20190633.	0.8	5
440	A High-Performance Systolic Array Accelerator Dedicated for CNN. , 2019, , .		5
441	Deep Learning Framework with Arbitrary Numerical Precision. , 2019, , .		2
442	Impact of CNNs Pooling Layer Implementation on FPGAs Accelerator Design. , 2019, , .		0
443	Hardware-Software Co-design Approach for Deep Learning Inference. , 2019, , .		4
444	Unrolling Ternary Neural Networks. ACM Transactions on Reconfigurable Technology and Systems, 2019, 12, 1-23.	2.5	26
445	Survey and Benchmarking of Machine Learning Accelerators. , 2019, , .		115
446	A Comparator Design Targeted towards Neural Nets. , 2019, , .		1
448	Multi-Precision Table-Addition Designs for Computing Nonlinear Functions in Deep Neural Networks. , 2019, , .		2
449	ALWANN: Automatic Layer-Wise Approximation of Deep Neural Network Accelerators without Retraining. , 2019, , .		71
450	A Uniform Modeling Methodology for Benchmarking DNN Accelerators. , 2019, , .		6
451	SPARE: Spiking Neural Network Acceleration Using ROM-Embedded RAMs as In-Memory-Computation Primitives. IEEE Transactions on Computers, 2019, 68, 1190-1200.	3.4	16
452	A 28-nm FD-SOI 8T Dual-Port SRAM for Low-Energy Image Processor With Selective Sourceline Drive Scheme. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1442-1453.	5.4	4
453	SynergyFlow. ACM Transactions on Design Automation of Electronic Systems, 2019, 24, 1-27.	2.6	5
454	A 4096-Neuron 1M-Synapse 3.8-pJ/SOP Spiking Neural Network With On-Chip STDP Learning and Sparse Weights in 10-nm FinFET CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 992-1002.	5.4	119

#	Article	IF	Citations
455	CONV-SRAM: An Energy-Efficient SRAM With In-Memory Dot-Product Computation for Low-Power Convolutional Neural Networks. IEEE Journal of Solid-State Circuits, 2019, 54, 217-230.	5.4	221
456	Promoting the Harmony between Sparsity and Regularity: A Relaxed Synchronous Architecture for Convolutional Neural Networks. IEEE Transactions on Computers, 2019, 68, 867-881.	3.4	3
457	SparCE: Sparsity Aware General-Purpose Core Extensions to Accelerate Deep Neural Networks. IEEE Transactions on Computers, 2019, 68, 912-925.	3.4	19
458	A Continuous-Time Replication Strategy for Efficient Multicast in Asynchronous NoCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 350-363.	3.1	8
459	A 34-FPS 698-GOP/s/W Binarized Deep Neural Network-Based Natural Scene Text Interpretation Accelerator for Mobile Edge Computing. IEEE Transactions on Industrial Electronics, 2019, 66, 7407-7416.	7.9	16
460	Emerging memory technologies for neuromorphic computing. Nanotechnology, 2019, 30, 032001.	2.6	62
461	Synthesizable Memory Arrays Based on Logic Gates for Subthreshold Operation in IoT. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 941-954.	5.4	18
462	Feedforward-Cutset-Free Pipelined Multiplyâ€“Accumulate Unit for the Machine Learning Accelerator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 138-146.	3.1	13
463	A Bi-layered Parallel Training Architecture for Large-Scale Convolutional Neural Networks. IEEE Transactions on Parallel and Distributed Systems, 2019, 30, 965-976.	5.6	145
464	A Robust Digital RRAM-Based Convolutional Block for Low-Power Image Processing and Learning Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 643-654.	5.4	39
465	Device and materials requirements for neuromorphic computing. Journal Physics D: Applied Physics, 2019, 52, 113001.	2.8	105
466	A 55-nm, 1.0â€“0.4V, 1.25-pJ/MAC Time-Domain Mixed-Signal Neuromorphic Accelerator With Stochastic Synapses for Reinforcement Learning in Autonomous Mobile Robots. IEEE Journal of Solid-State Circuits, 2019, 54, 75-87.	5.4	31
467	A 68-mw 2.2 Tops/w Low Bit Width and Multiplierless DCNN Object Detection Processor for Visually Impaired People. IEEE Transactions on Circuits and Systems for Video Technology, 2019, 29, 3444-3453.	8.3	18
468	Fundamentals and Literature Review. Computer Architecture and Design Methodologies, 2019, , 9-28.	0.8	0
469	Low power & mobile hardware accelerators for deep convolutional neural networks. The Integration VLSI Journal, 2019, 65, 110-127.	2.1	4
470	A Low-Power Deep Neural Network Online Learning Processor for Real-Time Object Tracking Application. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1794-1804.	5.4	37
471	Recent advances in convolutional neural network acceleration. Neurocomputing, 2019, 323, 37-51.	5.9	266
472	Joint Feature and Texture Coding: Toward Smart Video Representation via Front-End Intelligence. IEEE Transactions on Circuits and Systems for Video Technology, 2019, 29, 3095-3105.	8.3	29

#	Article	IF	Citations
473	UNPU: An Energy-Efficient Deep Neural Network Accelerator With Fully Variable Weight Bit Precision. IEEE Journal of Solid-State Circuits, 2019, 54, 173-185.	5.4	199
474	An Energy-Efficient FPGA-Based Deconvolutional Neural Networks Accelerator for Single Image Super-Resolution. IEEE Transactions on Circuits and Systems for Video Technology, 2020, 30, 281-295.	8.3	68
475	Boosting Convolutional Neural Networks Performance Based on FPGA Accelerator. Advances in Intelligent Systems and Computing, 2020, , 509-517.	0.6	18
476	Toward Massive Machine Type Communications in Ultra-Dense Cellular IoT Networks: Current Issues and Machine Learning-Assisted Solutions. IEEE Communications Surveys and Tutorials, 2020, 22, 426-471.	39.4	256
477	Compact and Computationally Efficient Representation of Deep Neural Networks. IEEE Transactions on Neural Networks and Learning Systems, 2020, 31, 772-785.	11.3	46
478	A Resource-Efficient Multiplierless Systolic Array Architecture for Convolutions in Deep Networks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 370-374.	3.0	16
479	Multiple classifiers fusion and CNN feature extraction for handwritten digits recognition. Granular Computing, 2020, 5, 411-418.	8.0	70
480	Processing Near Sensor Architecture in Mixed-Signal Domain With CMOS Image Sensor of Convolutional-Kernel-Readout Method. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 389-400.	5.4	28
481	Fast and Efficient Convolutional Accelerator for Edge Computing. IEEE Transactions on Computers, 2020, 69, 138-152.	3.4	37
482	Rethinking the performance comparison between SNNS and ANNS. Neural Networks, 2020, 121, 294-307.	5.9	131
483	A Survey of Coarse-Grained Reconfigurable Architecture and Design. ACM Computing Surveys, 2020, 52, 1-39.	23.0	119
484	Vesti: Energy-Efficient In-Memory Computing Accelerator for Deep Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 48-61.	3.1	32
485	A Training-Efficient Hybrid-Structured Deep Neural Network With Reconfigurable Memristive Synapses. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 62-75.	3.1	22
486	An Improved Low-Power Coding for Serial Network-On-Chip Links. Circuits, Systems, and Signal Processing, 2020, 39, 1896-1919.	2.0	7
487	SemiMap: A Semi-Folded Convolution Mapping for Speed-Overhead Balance on Crossbars. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 117-130.	2.7	15
488	FPGA-Based Implementation of a Real-Time Object Recognition System Using Convolutional Neural Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 755-759.	3.0	23
489	Balancing Computation Loads and Optimizing Input Vector Loading in LSTM Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1889-1901.	2.7	5
490	An Energy-Efficient Deep Convolutional Neural Network Inference Processor With Enhanced Output Stationary Dataflow in 65-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 87-100.	3.1	40

#	Article	IF	Citations
491	New Flexible Multiple-Precision Multiply-Accumulate Unit for Deep Neural Network Training and Inference. IEEE Transactions on Computers, 2020, 69, 26-38.	3.4	26
492	Asymptotic Soft Filter Pruning for Deep Convolutional Neural Networks. IEEE Transactions on Cybernetics, 2020, 50, 3594-3604.	9.5	111
493	Implementation of DNNs on IoT devices. Neural Computing and Applications, 2020, 32, 1327-1356.	5.6	14
494	Data clustering for efficient approximate computing. Design Automation for Embedded Systems, 2020, 24, 3-22.	1.0	2
495	A 12.08-TOPS/W All-Digital Time-Domain CNN Engine Using Bi-Directional Memory Delay Lines for Energy Efficient Edge Computing. IEEE Journal of Solid-State Circuits, 2020, 55, 60-75.	5.4	42
496	A streaming architecture for Convolutional Neural Networks based on layer operations chaining. Journal of Real-Time Image Processing, 2020, 17, 1715-1733.	3.5	9
497	Gain-Cell Embedded DRAMs: Modeling and Design Space. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 646-659.	3.1	6
498	Magnetic Domain Wall Based Synaptic and Activation Function Generator for Neuromorphic Accelerators. Nano Letters, 2020, 20, 1033-1040.	9.1	72
499	A novel hardware-oriented ultra-high-speed object detection algorithm based on convolutional neural network. Journal of Real-Time Image Processing, 2020, 17, 1703-1714.	3.5	6
500	A highly stable reliable SRAM cell design for low power applications. Microelectronics Reliability, 2020, 105, 113503.	1.7	39
501	OPTIMO: A 65-nm 279-GOPS/W 16-b Programmable Spatial-Array Processor with On-Chip Network for Solving Distributed Optimizations via the Alternating Direction Method of Multipliers. IEEE Journal of Solid-State Circuits, 2020, 55, 629-638.	5.4	2
502	Enabling Timing Error Resilience for Low-Power Systolic-Array Based Deep Learning Accelerators. IEEE Design and Test, 2020, 37, 93-102.	1.2	10
503	Deep In-Memory Architectures for Machine Learningâ€“Accuracy Versus Efficiency Trade-Offs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1627-1639.	5.4	16
504	Ring-mesh: a scalable and high-performance approach for manycore accelerators. Journal of Supercomputing, 2020, 76, 6720-6752.	3.6	2
505	ICNN. Transactions on Embedded Computing Systems, 2019, 18, 1-27.	2.9	9
506	Mapping Spiking Neural Networks to Neuromorphic Hardware. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 76-86.	3.1	75
507	PIMBALL. Transactions on Architecture and Code Optimization, 2019, 16, 1-26.	2.0	24
508	Res-DNN: A Residue Number System-Based DNN Accelerator Unit. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 658-671.	5.4	37

#	Article	IF	Citations
509	VWA: Hardware Efficient Vectorwise Accelerator for Convolutional Neural Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 145-154.	5.4	31
510	A Systolic Dataflow Based Accelerator for CNNs. , 2020, , .		10
511	High-Speed Power-Efficient Coarse-Grained Convolver Architecture using Depth-First Compression Scheme. , 2020, , .		2
512	Flash Based In-Memory Multiply-Accumulate Realisation: A Theoretical Study. , 2020, , .		1
513	CRIMSON: Compute-Intensive Loop Acceleration by Randomized Iterative Modulo Scheduling and Optimized Mapping on CGRAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3300-3310.	2.7	13
514	Dustâ€Sized Highâ€Powerâ€Density Photovoltaic Cells on Si and SOI Substrates for Waferâ€Levelâ€Packaged Small Edge Computers. Advanced Materials, 2020, 32, e2004573.	21.0	7
515	A Two-way SRAM Array based Accelerator for Deep Neural Network On-chip Training. , 2020, , .		21
516	Towards Efficient On-Chip Learning using Equilibrium Propagation. , 2020, , .		2
517	Automated optimization for memoryâ€efficient highâ€performance deep neural network accelerators. ETRI Journal, 2020, 42, 505-517.	2.0	8
518	VLSI Design of Tree-Based Inference for Low-Power Learning Applications. , 2020, , .		7
519	PulseDL: A reconfigurable deep learning array processor dedicated to pulse characterization for high energy physics detectors. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2020, 978, 164420.	1.6	5
520	Resistive Crossbars as Approximate Hardware Building Blocks for Machine Learning: Opportunities and Challenges. Proceedings of the IEEE, 2020, 108, 2276-2310.	21.3	55
521	A 2.9â€“33.0 TOPS/W Reconfigurable 1-D/2-D Compute-Near-Memory Inference Accelerator in 10-nm FinFET CMOS. IEEE Solid-State Circuits Letters, 2020, 3, 118-121.	2.0	4
522	Analysis of a Pipelined Architecture for Sparse DNNs on Embedded Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1993-2003.	3.1	10
523	Low-Complexity On-Demand Reconstruction for Compressively Sensed Problematic Signals. IEEE Transactions on Signal Processing, 2020, 68, 4094-4107.	5.3	3
524	aCortex: An Energy-Efficient Multipurpose Mixed-Signal Inference Accelerator. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 98-106.	1.5	5
525	An Updated Survey of Efficient Hardware Architectures for Accelerating Deep Convolutional Neural Networks. Future Internet, 2020, 12, 113.	3.8	111
526	An 8.93 TOPS/W LSTM Recurrent Neural Network Accelerator Featuring Hierarchical Coarse-Grain Sparsity for On-Device Speech Recognition. IEEE Journal of Solid-State Circuits, 2020, 55, 1877-1887.	5.4	36

#	Article	IF	Citations
527	Base-Reconfigurable Segmented Logarithmic Quantization and Hardware Design for Deep Neural Networks. Journal of Signal Processing Systems, 2020, 92, 1263-1276.	2.1	8
528	F-DNA: Fast Convolution Architecture for Deconvolutional Network Acceleration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1867-1880.	3.1	11
529	Analog Circuits to Accelerate the Relaxation Process in the Equilibrium Propagation Algorithm. , 2020, , .		4
530	Exploring GPU acceleration of Deep Neural Networks using Block Circulant Matrices. Parallel Computing, 2020, 100, 102701.	2.1	6
531	A 30â€¯MB re-configurable convolutional neural network processor for high-performance and energy-efficient operation. Materials Today: Proceedings, 2020, , .	1.8	0
532	60â€4: Implementation and Optimization of FSRCNNâ€s Algorithm Based on SDSoC Platform. Digest of Technical Papers SID International Symposium, 2020, 51, 901-904.	0.3	1
533	MINT: Mixed-Precision RRAM-Based IN-Memory Training Architecture. , 2020, , .		15
534	An In-Flash Binary Neural Network Accelerator with SLC NAND Flash Array. , 2020, , .		5
535	A Multi-grained Reconfigurable Accelerator for Approximate Computing. , 2020, , .		7
536	CASH-RAM: Enabling In-Memory Computations for Edge Inference Using Charge Accumulation and Sharing in Standard 8T-SRAM Arrays. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 295-305.	3.6	16
537	Heterogeneous Distributed SRAM Configuration for Energy-Efficient Deep CNN Accelerators. , 2020, , .		0
538	Always-On 674Î¼W@4GOP/s Error Resilient Binary Neural Networks With Aggressive SRAM Voltage Scaling on a 22-nm IoT End-Node. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3905-3918.	5.4	23
539	A Survey of Stochastic Computing Neural Networks for Machine Learning Applications. IEEE Transactions on Neural Networks and Learning Systems, 2021, 32, 2809-2824.	11.3	86
540	DNN-Chip Predictor: An Analytical Performance Predictor for DNN Accelerators with Various Dataflows and Hardware Architectures. , 2020, , .		25
541	CAxCNN: Towards the Use of Canonic Sign Digit Based Approximation for Hardware-Friendly Convolutional Neural Networks. IEEE Access, 2020, 8, 127014-127021.	4.2	13
542	A Survey on Coarse-Grained Reconfigurable Architectures From a Performance Perspective. IEEE Access, 2020, 8, 146719-146743.	4.2	70
543	CSCMAC - Cyclic Sparsely Connected Neural Network Manycore Accelerator. , 2020, , .		1
544	Reconfigurable Stream-based Tensor Unit with Variable-Precision Posit Arithmetic. , 2020, , .		4

#	Article	IF	Citations
545	Lupulus: A Flexible Hardware Accelerator for Neural Networks. , 2020, , .		0
546	Enhancing the Utilization of Dot-Product Engines in Deep Learning Accelerators. , 2020, , .		0
547	Nanoscale Side-Contact Enabled Three Terminal Pr_{0.7}Ca_{0.3}MnO₃ Resistive Random Access Memory for In-Memory Computing. IEEE Electron Device Letters, 2020, 41, 1344-1347.	3.9	7
548	A 1-Mbit Fully Logic-Compatible 3T Gain-Cell Embedded DRAM in 16-nm FinFET. IEEE Solid-State Circuits Letters, 2020, 3, 110-113.	2.0	8
549	dMazeRunner: Optimizing Convolutions on Dataflow Accelerators. , 2020, , .		9
550	RecNMP: Accelerating Personalized Recommendation with Near-Memory Processing. , 2020, , .		85
551	Defect Characterization of Spintronic-based Neuromorphic Circuits. , 2020, , .		3
552	An Energy-Efficient Accelerator Architecture with Serial Accumulation Dataflow for Deep CNNs. , 2020, , .		3
553	SmartExchange: Trading Higher-cost Memory Storage/Access for Lower-cost Computation. , 2020, , .		28
554	MEM-OPT: A Scheduling and Data Re-Use System to Optimize On-Chip Memory Usage for CNNs On-Board FPGAs. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 335-347.	3.6	16
555	Refresh Power Reduction of DRAMs in DNN Systems Using Hybrid Voting and ECC Method. , 2020, , .		0
556	A Convolutional Neural Network Accelerator Architecture with Fine-Granular Mixed Precision Configurability. , 2020, , .		7
557	Exploiting Zero Data to Reduce Register File and Execution Unit Dynamic Power Consumption in GPGPUs. , 2020, , .		3
558	Imperceptible Misclassification Attack on Deep Learning Accelerator by Glitch Injection. , 2020, , .		22
559	Factored Radix-8 Systolic Array for Tensor Processing. , 2020, , .		8
560	Input-Dependent Edge-Cloud Mapping of Recurrent Neural Networks Inference. , 2020, , .		6
561	Sparsity-Aware Deep Learning Accelerator Design Supporting CNN and LSTM Operations. , 2020, , .		4
562	Arithmetic Precision Reconfigurable Convolution Neural Network Accelerator. , 2020, , .		0

#	Article	IF	Citations
563	An Accelerator Design Using a MTCA Decomposition Algorithm for CNNs. Sensors, 2020, 20, 5558.	3.8	5
564	Training DNN IoT Applications for Deployment On Analog NVM Crossbars. , 2020, , .		3
565	Efficient Scheduling of Irregular Network Structures on CNN Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3408-3419.	2.7	16
566	Soft errors in DNN accelerators: A comprehensive review. Microelectronics Reliability, 2020, 115, 113969.	1.7	41
567	Roofline-Model-Based Design Space Exploration for Dataflow Techniques of CNN Accelerators. IEEE Access, 2020, 8, 172509-172523.	4.2	12
568	PCNN: Pattern-based Fine-Grained Regular Pruning Towards Optimizing CNN Accelerators. , 2020, , .		12
569	A CycleGAN Accelerator for Unsupervised Learning on Mobile Devices. , 2020, , .		3
570	WinDConv: A Fused Datapath CNN Accelerator for Power-Efficient Edge Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4278-4289.	2.7	3
571	Dynamically Reconfigurable Deep Learning for Efficient Video Processing in Smart IoT Systems. , 2020, , .		4
572	INVITED: Computation on Sparse Neural Networks and its Implications for Future Hardware. , 2020, , .		9
573	DRMap: A Generic DRAM Data Mapping Policy for Energy-Efficient Processing of Convolutional Neural Networks. , 2020, , .		10
574	Recent Progress on Memristive Convolutional Neural Networks for Edge Intelligence. Advanced Intelligent Systems, 2020, 2, 2000114.	6.1	19
575	Design of a Sparsity-Aware Reconfigurable Deep Learning Accelerator Supporting Various Types of Operations. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 376-387.	3.6	16
576	High-Throughput In-Memory Computing for Binary Deep Neural Networks With Monolithically Integrated RRAM and 90-nm CMOS. IEEE Transactions on Electron Devices, 2020, 67, 4185-4192.	3.0	92
577	Chronos Link: A QDI Interconnect for Modern SoCs. , 2020, , .		1
578	An Elastic Neural Network Toward Multi-Grained Re-configurable Accelerator. , 2020, , .		0
579	Hardware design and the competency awareness of a neural network. Nature Electronics, 2020, 3, 514-523.	26.0	14
580	ADIC: Anomaly Detection Integrated Circuit in 65-nm CMOS Utilizing Approximate Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2518-2529.	3.1	6

#	Article	IF	Citations
581	An Overview of Efficient Interconnection Networks for Deep Neural Network Accelerators. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 268-282.	3.6	46
582	Inâ€Memory Vectorâ€Matrix Multiplication in Monolithic Complementary Metalâ€“Oxideâ€“Semiconductorâ€Memristor Integrated Circuits: Design Choices, Challenges, and Perspectives. Advanced Intelligent Systems, 2020, 2, 2000115.	6.1	100
583	Efficient Decoder Reduction for a Variety of Encoder-Decoder Problems. IEEE Access, 2020, 8, 169444-169455.	4.2	0
584	APNAS: Accuracy-and-Performance-Aware Neural Architecture Search for Neural Hardware Accelerators. IEEE Access, 2020, 8, 165319-165334.	4.2	21
585	How to Evaluate Deep Neural Network Processors: TOPS/W (Alone) Considered Harmful. IEEE Solid-State Circuits Magazine, 2020, 12, 28-41.	0.4	40
586	CRIME: Input-Dependent Collaborative Inference for Recurrent Neural Networks. IEEE Transactions on Computers, 2020, , 1-1.	3.4	10
587	Flexible Multi-Precision Accelerator Design for Deep Convolutional Neural Networks Considering Both Data Computation and Communication. , 2020, , .		2
588	Attention-Based Activation Pruning to Reduce Data Movement in Real-Time AI: A Case-Study on Local Motion Planning in Autonomous Vehicles. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 306-319.	3.6	11
589	The Hardware and Algorithm Co-Design for Energy-Efficient DNN Processor on Edge/Mobile Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3458-3470.	5.4	25
590	Exploiting Retraining-Based Mixed-Precision Quantization for Low-Cost DNN Accelerator Design. IEEE Transactions on Neural Networks and Learning Systems, 2021, 32, 2925-2938.	11.3	13
591	A Systematic Study of Tiny YOLO3 Inference: Toward Compact Brainware Processor With Less Memory and Logic Gate. IEEE Access, 2020, 8, 142931-142955.	4.2	15
592	Analog Vector-Matrix Multiplier Based on Programmable Current Mirrors for Neural Network Integrated Circuits. IEEE Access, 2020, 8, 203525-203537.	4.2	20
593	Hardware-Based Real-Time Deep Neural Network Lossless Weights Compression. IEEE Access, 2020, 8, 205051-205060.	4.2	5
594	Hardware and Software Optimizations for Accelerating Deep Neural Networks: Survey of Current Trends, Challenges, and the Road Ahead. IEEE Access, 2020, 8, 225134-225180.	4.2	91
595	Hardware Implementation of Deep Network Accelerators Towards Healthcare and Biomedical Applications. IEEE Transactions on Biomedical Circuits and Systems, 2020, 14, 1138-1159.	4.0	93
596	A High-Accuracy Hardware-Efficient Multiplyâ€“Accumulate (MAC) Unit Based on Dual-Mode Truncation Error Compensation for CNNs. IEEE Access, 2020, 8, 214716-214731.	4.2	4
597	AWB-GCN: A Graph Convolutional Network Accelerator with Runtime Workload Rebalancing. , 2020, , .		132
598	An Energy-Efficient Silicon Photonic-Assisted Deep Learning Accelerator for Big Data. Wireless Communications and Mobile Computing, 2020, 2020, 1-11.	1.2	4

#	Article	IF	Citations
599	Bitstream-Based Neural Network for Scalable, Efficient, and Accurate Deep Learning Hardware. Frontiers in Neuroscience, 2020, 14, 543472.	2.8	5
600	A Novel Multi-Scale Feature Fusion Method for Region Proposal Network in Fast Object Detection. International Journal of Data Warehousing and Mining, 2020, 16, 132-145.	0.6	8
601	Challenges and Opportunities in Near-Threshold DNN Accelerators around Timing Errors. Journal of Low Power Electronics and Applications, 2020, 10, 33.	2.0	5
602	Everything Leaves Footprints: Hardware Accelerated Intermittent Deep Inference. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3479-3491.	2.7	23
603	SuperSlash: A Unified Design Space Exploration and Model Compression Methodology for Design of Deep Learning Accelerators With Reduced Off-Chip Memory Access Volume. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4191-4204.	2.7	7
604	Deep Neural Networks Characterization Framework for Efficient Implementation on Embedded Systems. , 2020, , .		3
605	Zebra: Memory Bandwidth Reduction for CNN Accelerators with Zero Block Regularization of Activation Maps. , 2020, , .		1
606	Efficient Accelerator for Dilated and Transposed Convolution with Decomposition. , 2020, , .		14
607	A Model-to-Circuit Compiler for Evaluation of DNN Accelerators based on Systolic Arrays and Multibit Emerging Memories. , 2020, , .		4
608	A Fifo Based Accelerator for Convolutional Neural Networks. , 2020, , .		4
609	A 2.17-mW Acoustic DSP Processor With CNN-FFT Accelerators for Intelligent Hearing Assistive Devices. IEEE Journal of Solid-State Circuits, 2020, 55, 2247-2258.	5.4	8
610	Asymmetric Resilience: Exploiting Task-Level Idempotency for Transient Error Recovery in Accelerator-Based Systems. , 2020, , .		14
611	A 44.1TOPS/W Precision-Scalable Accelerator for Quantized Neural Networks in 28nm CMOS. , 2020, , .		6
612	Deep Convolutional Neural Network Accelerator Featuring Conditional Computing and Low External Memory Access. , 2020, , .		5
613	Communication Lower Bound in Convolution Accelerators. , 2020, , .		21
614	Convergence of Artificial Intelligence and the Internet of Things. Internet of Things, 2020, , .	1.7	11
615	CRAM: Collocated SRAM and DRAM With In-Memory Computing-Based Denoising and Filling for Neuromorphic Vision Sensors in 65 nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 816-820.	3.0	4
616	In-memory computing to break the memory wall*. Chinese Physics B, 2020, 29, 078504.	1.4	28

#	Article	IF	Citations
617	A Relaxed Quantization Training Method for Hardware Limitations of Resistive Random Access Memory (ReRAM)-Based Computing-in-Memory. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 45-52.	1.5	8
618	Implementation of energyâ€efficient fast convolution algorithm for deep convolutional neural networks based on FPGA. Electronics Letters, 2020, 56, 485-488.	1.0	4
619	Review of prominent strategies for mapping CNNs onto embedded systems. IEEE Latin America Transactions, 2020, 18, 971-982.	1.6	12
620	SSM: a high-performance scheme for in situ training of imprecise memristor neural networks. Neurocomputing, 2020, 407, 270-280.	5.9	12
621	PIXEL: Photonic Neural Network Accelerator. , 2020, , .		27
622	A Stride-Based Convolution Decomposition Method to Stretch CNN Acceleration Algorithms for Efficient and Flexible Hardware Implementation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3007-3020.	5.4	22
623	A Programmable Heterogeneous Microprocessor Based on Bit-Scalable In-Memory Computing. IEEE Journal of Solid-State Circuits, 2020, 55, 2609-2621.	5.4	89
624	MAESTRO: A Data-Centric Approach to Understand Reuse, Performance, and Hardware Cost of DNN Mappings. IEEE Micro, 2020, 40, 20-29.	1.8	75
625	A Coarse-Grained Dual-Convolver Based CNN Accelerator with High Computing Resource Utilization. , 2020, , .		4
626	Hardware Implementation of Neural Self-Interference Cancellation. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 204-216.	3.6	26
627	NeuPart: Using Analytical Models to Drive Energy-Efficient Partitioning of CNN Computations on Cloud-Connected Mobile Clients. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1844-1857.	3.1	10
628	Energy-Efficient Accelerator Design with 3D-SRAM and Hierarchical Interconnection Architecture for Compact Sparse CNNs. , 2020, , .		5
629	C3SRAM: An In-Memory-Computing SRAM Macro Based on Robust Capacitive Coupling Computing Mechanism. IEEE Journal of Solid-State Circuits, 2020, 55, 1888-1897.	5.4	144
630	A Precision-Scalable Energy-Efficient Convolutional Neural Network Accelerator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3484-3497.	5.4	18
631	The Development of Silicon for AI: Different Design Approaches. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4719-4732.	5.4	10
632	A NoC-based simulator for design and evaluation of deep neural networks. Microprocessors and Microsystems, 2020, 77, 103145.	2.8	8
633	Multi-Resolution Siamese Networks for One-Shot Learning. , 2020, , .		3
634	Zero Block Caching for CNN Applications Running on a Vision DSP. , 2020, , .		0

#	Article	IF	Citations
635	A Mathematical Approach Towards Quantization of Floating Point Weights in Low Power Neural Networks. , 2020, , .		4
636	A^3: Accelerating Attention Mechanisms in Neural Networks with Approximation. , 2020, , .		69
637	FPGA based convolution and memory architecture for Convolutional Neural Network. , 2020, , .		1
638	CyNAPSE: A Low-power Reconfigurable Neural Inference Accelerator for Spiking Neural Networks. Journal of Signal Processing Systems, 2020, 92, 907-929.	2.1	2
639	A 1.5 mW Programmable Acoustic Signal Processor for Hearing Assistive Devices With Speech Intelligibility Enhancement. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4984-4993.	5.4	3
640	Moving Deep Learning to the Edge. Algorithms, 2020, 13, 125.	2.1	48
641	Automated design of error-resilient and hardware-efficient deep neural networks. Neural Computing and Applications, 2020, 32, 18327-18345.	5.6	21
642	Pre-defined Sparsity for Low-Complexity Convolutional Neural Networks. IEEE Transactions on Computers, 2020, , 1-1.	3.4	29
643	Addressing Irregularity in Sparse Neural Networks through a Cooperative Software/Hardware Approach. IEEE Transactions on Computers, 2020, , 1-1.	3.4	3
644	Model Compression and Hardware Acceleration for Neural Networks: A Comprehensive Survey. Proceedings of the IEEE, 2020, 108, 485-532.	21.3	441
645	Systolic Tensor Array: An Efficient Structured-Sparse GEMM Accelerator for Mobile CNN Inference. IEEE Computer Architecture Letters, 2020, 19, 34-37.	1.5	46
647	Bio-mimetic synaptic plasticity and learning in a sub-500ÂmV Cu/SiO2/W memristor. Microelectronic Engineering, 2020, 226, 111290.	2.4	11
648	Current-Based Data-Retention-Time Characterization of Gain-Cell Embedded DRAMs Across the Design and Variations Space. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1207-1217.	5.4	8
649	An Artificial Neural Network Processor With a Custom Instruction Set Architecture for Embedded Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 5200-5210.	5.4	10
650	Analysis and Solution of CNN Accuracy Reduction over Channel Loop Tiling. , 2020, , .		0
651	FPGA-Based Memristor Emulator Circuit for Binary Convolutional Neural Networks. IEEE Access, 2020, 8, 117736-117745.	4.2	3
652	Efficient Hardware Architectures for 1D- and MD-LSTM Networks. Journal of Signal Processing Systems, 2020, 92, 1219-1245.	2.1	9
653	ESSA: An energy-Aware bit-Serial streaming deep convolutional neural network accelerator. Journal of Systems Architecture, 2020, 111, 101831.	4.3	10

#	Article	IF	Citations
654	Binary neural networks: A survey. Pattern Recognition, 2020, 105, 107281.	8.1	276
655	CREMON: Cryptography Embedded on the Convolutional Neural Network Accelerator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3337-3341.	3.0	6
656	Architecture, challenges and applications of dynamic reconfigurable computing. Journal of Semiconductors, 2020, 41, 021401.	3.7	7
657	A survey of neural network accelerator with software development environments. Journal of Semiconductors, 2020, 41, 021403.	3.7	5
658	A Novel Architecture for Early Detection of Negative Output Features in Deep Neural Network Accelerators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3332-3336.	3.0	6
659	Tianjic: A Unified and Scalable Chip Bridging Spike-Based and Continuous Neural Computation. IEEE Journal of Solid-State Circuits, 2020, 55, 2228-2246.	5.4	78
660	Exploring Efficient Acceleration Architecture for Winograd-Transformed Transposed Convolution of GANs on FPGAs. Electronics (Switzerland), 2020, 9, 286.	3.1	13
661	SLIM: Simultaneous Logic-in-Memory Computing Exploiting Bilayer Analog OxRAM Devices. Scientific Reports, 2020, 10, 2567.	3.3	1,186
662	Accelerating hybrid and compact neural networks targeting perception and control domains with coarse-grained dataflow reconfiguration. Journal of Semiconductors, 2020, 41, 022401.	3.7	5
663	Reconfigurable and Low-Complexity Accelerator for Convolutional and Generative Networks Over Finite Fields. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4894-4907.	2.7	10
664	Silicon Photonics Codesign for Deep Learning. Proceedings of the IEEE, 2020, 108, 1261-1282.	21.3	52
665	Domain Wall Memory-Based Design of Deep Neural Network Convolutional Layers. IEEE Access, 2020, 8, 19783-19798.	4.2	5
666	GAAS: An Efficient Group Associated Architecture and Scheduler Module for Sparse CNN Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5170-5182.	2.7	2
667	Soft Error Resilience of Deep Residual Networks for Object Recognition. IEEE Access, 2020, 8, 19490-19503.	4.2	37
668	A 0.32â€“128 TOPS, Scalable Multi-Chip-Module-Based Deep Neural Network Inference Accelerator With Ground-Referenced Signaling in 16 nm. IEEE Journal of Solid-State Circuits, 2020, 55, 920-932.	5.4	57
669	Fully hardware-implemented memristor convolutional neural network. Nature, 2020, 577, 641-646.	27.8	1,198
670	Deep In-memory Architectures for Machine Learning. , 2020, , .		7
671	Nanoscale resistive switching devices for memory and computing applications. Nano Research, 2020, 13, 1228-1243.	10.4	91

#	Article	IF	Citations
672	CoNNaâ€“Hardware accelerator for compressed convolutional neural networks. Microprocessors and Microsystems, 2020, 73, 102991.	2.8	13
673	XNOR-SRAM: In-Memory Computing SRAM Macro for Binary/Ternary Deep Neural Networks. IEEE Journal of Solid-State Circuits, 2020, , 1-11.	5.4	189
674	A Survey of Accelerator Architectures for Deep Neural Networks. Engineering, 2020, 6, 264-274.	6.7	174
675	An Approximate Memory Architecture for Energy Saving in Deep Learning Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1588-1601.	5.4	28
676	Prediction of Gas Concentration Using Gated Recurrent Neural Networks. , 2020, , .		10
677	AccPar: Tensor Partitioning for Heterogeneous Deep Learning Accelerators. , 2020, , .		24
678	The Architectural Implications of Facebook's DNN-Based Personalized Recommendation. , 2020, , .		113
679	Conductive-bridging random-access memories for emerging neuromorphic computing. Nanoscale, 2020, 12, 14339-14368.	5.6	46
680	EFLOPS: Algorithm and System Co-Design for a High Performance Distributed Training Platform. , 2020, , .		21
681	Dual Dynamic Inference: Enabling More Efficient, Adaptive, and Controllable Deep Inference. IEEE Journal on Selected Topics in Signal Processing, 2020, 14, 623-633.	10.8	39
682	NS-CIM: A Current-Mode Computation-in-Memory Architecture Enabling Near-Sensor Processing for Intelligent IoT Vision Nodes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2909-2922.	5.4	25
683	PreVIous: A Methodology for Prediction of Visual Inference Performance on IoT Devices. IEEE Internet of Things Journal, 2020, 7, 9227-9240.	8.7	15
684	An Efficient Accelerator for Multiple Convolutions From the Sparsity Perspective. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, , 1-5.	3.1	10
685	Variances-constrained weighted extreme learning machine for imbalanced classification. Neurocomputing, 2020, 403, 45-52.	5.9	15
686	Swallow: A Versatile Accelerator for Sparse Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4881-4893.	2.7	11
687	Machine learning in digital health, recent trends, and ongoing challenges. , 2020, , 121-148.		1
688	AIM: Annealing in Memory for Vision Applications. Symmetry, 2020, 12, 480.	2.2	1
689	Fast Algorithms for Quaternion-Valued Convolutional Neural Networks. IEEE Transactions on Neural Networks and Learning Systems, 2021, 32, 457-462.	11.3	10

#	Article	IF	Citations
690	PermCNN: Energy-Efficient Convolutional Neural Network Hardware Architecture With Permuted Diagonal Structure. IEEE Transactions on Computers, 2021, 70, 163-173.	3.4	15
691	UL-CNN: An Ultra-Lightweight Convolutional Neural Network Aiming at Flash-Based Computing-In-Memory Architecture for Pedestrian Recognition. Journal of Circuits, Systems and Computers, 2021, 30, 2150022.	1.5	4
692	An On-Chip Binary-Weight Convolution CMOS Image Sensor for Neural Networks. IEEE Transactions on Industrial Electronics, 2021, 68, 7567-7576.	7.9	11
693	MAHASIM: Machine-Learning Hardware Acceleration Using a Software-Defined Intelligent Memory System. Journal of Signal Processing Systems, 2021, 93, 659-675.	2.1	1
694	A Dynamic Timing Enhanced DNN Accelerator With Compute-Adaptive Elastic Clock Chain Technique. IEEE Journal of Solid-State Circuits, 2021, 56, 55-65.	5.4	9
695	Enhancing the Utilization of Processing Elements in Spatial Deep Neural Network Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1947-1951.	2.7	5
696	A dynamic CNN pruning method based on matrix similarity. Signal, Image and Video Processing, 2021, 15, 381-389.	2.7	16
697	Merged Logic and Memory Fabrics for Accelerating Machine Learning Workloads. IEEE Design and Test, 2021, 38, 39-68.	1.2	10
698	An Edge 3D CNN Accelerator for Low-Power Activity Recognition. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 918-930.	2.7	10
699	LrGAN: A Compact and Energy Efficient PIM-Based Architecture for GAN Training. IEEE Transactions on Computers, 2021, 70, 1427-1442.	3.4	1
700	In-memory Learning with Analog Resistive Switching Memory: A Review and Perspective. Proceedings of the IEEE, 2021, 109, 14-42.	21.3	96
701	Accelerating Deep Convolutional Neural Network base on stochastic computing. The Integration VLSI Journal, 2021, 76, 113-121.	2.1	11
702	Accelerating CNN Inference on ASICs: A Survey. Journal of Systems Architecture, 2021, 113, 101887.	4.3	44
703	Evaluating and analyzing the energy efficiency of CNN inference on highâ€performance GPU. Concurrency Computation Practice and Experience, 2021, 33, e6064.	2.2	15
704	Partial-neurons-based state estimation for delayed neural networks with state-dependent noises under redundant channels. Information Sciences, 2021, 547, 931-944.	6.9	11
705	Design of Convolutional Neural Network with Cuckoo Search Algorithm for Super-Resolution UHD Systems on FPGA. Journal of Circuits, Systems and Computers, 2021, 30, 2150155.	1.5	1
706	High Performance CNN Accelerators Based on Hardware and Algorithm Co-Optimization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 250-263.	5.4	48
707	MOSDA: On-Chip Memory Optimized Sparse Deep Neural Network Accelerator With Efficient Index Matching. IEEE Open Journal of Circuits and Systems, 2021, 2, 144-155.	1.9	1

#	Article	IF	Citations
708	ConvAix: An Application-Specific Instruction-Set Processor for the Efficient Acceleration of CNNs. IEEE Open Journal of Circuits and Systems, 2021, 2, 3-15.	1.9	9
709	Flash Memory Array for Efficient Implementation of Deep Neural Networks. Advanced Intelligent Systems, 2021, 3, 2000161.	6.1	14
710	Spaceâ€address decoupled scratchpad memory management for neural network accelerators. Concurrency Computation Practice and Experience, 2021, 33, e6046.	2.2	1
711	An Energy-Efficient Deep Convolutional Neural Network Accelerator Featuring Conditional Computing and Low External Memory Access. IEEE Journal of Solid-State Circuits, 2021, 56, 803-813.	5.4	11
712	A 510-nW Wake-Up Keyword-Spotting Chip Using Serial-FFT-Based MFCC and Binarized Depthwise Separable CNN in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2021, 56, 151-164.	5.4	42
713	Accuracy-Guaranteed Collaborative DNN Inference in Industrial IoT via Deep Reinforcement Learning. IEEE Transactions on Industrial Informatics, 2021, 17, 4988-4998.	11.3	58
714	A Throughput-Optimized Channel-Oriented Processing Element Array for Convolutional Neural Networks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 752-756.	3.0	7
715	Modeling Data Reuse in Deep Neural Networks by Taking Data-Types into Cognizance. IEEE Transactions on Computers, 2021, 70, 1526-1538.	3.4	8
716	SeFAct2: Selective Feature Activation for Energy-Efficient CNNs Using Optimized Thresholds. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1423-1436.	2.7	1
717	Layer-Specific Optimization for Mixed Data Flow With Mixed Precision in FPGA Design for CNN-Based Object Detectors. IEEE Transactions on Circuits and Systems for Video Technology, 2021, 31, 2450-2464.	8.3	42
718	M2DA: A Low-Complex Design Methodology for Convolutional Neural Network Exploiting Data Symmetry and Redundancy. Circuits, Systems, and Signal Processing, 2021, 40, 1542-1567.	2.0	3
719	FantastIC4: A Hardware-Software Co-Design Approach for Efficiently Running 4Bit-Compact Multilayer Perceptrons. IEEE Open Journal of Circuits and Systems, 2021, 2, 407-419.	1.9	7
720	SLID: Exploiting Spatial Locality in Input Data as a Computational Reuse Method for Efficient CNN. IEEE Access, 2021, 9, 57179-57187.	4.2	3
721	Effective Spare Line Allocation Built-in Redundancy Analysis With Base Common Spare for Yield Improvement of 3D Memory. IEEE Access, 2021, 9, 76716-76729.	4.2	0
722	Hardware-Enabled Efficient Data Processing With Tensor-Train Decomposition. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 372-385.	2.7	3
723	Polymorphic Accelerators for Deep Neural Networks. IEEE Transactions on Computers, 2022, 71, 534-546.	3.4	7
724	A Hierarchical K-Means-Assisted Scenario-Aware Reconfigurable Convolutional Neural Network. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 176-188.	3.1	3
725	Efficiency Versus Accuracy: A Review of Design Techniques for DNN Hardware Accelerators. IEEE Access, 2021, 9, 9785-9799.	4.2	18

#	Article	IF	Citations
726	Introduction to hardware accelerator systems for artificial intelligence and machine learning. Advances in Computers, 2021, 122, 1-21.	1.6	5
727	The Why, What, and How of Artificial General Intelligence Chip Development. IEEE Transactions on Cognitive and Developmental Systems, 2022, 14, 333-347.	3.8	13
728	Highly-Parallel Hardwired Deep Convolutional Neural Network for 1-ms Dual-Hand Tracking. IEEE Transactions on Circuits and Systems for Video Technology, 2022, 32, 8192-8203.	8.3	5
729	A Novel CONV Acceleration Strategy Based on Logical PE Set Segmentation for Row Stationary Dataflow. IEEE Transactions on Computers, 2021, , 1-1.	3.4	1
730	CNN Inference Using a Preprocessing Precision Controller and Approximate Multipliers With Various Precisions. IEEE Access, 2021, 9, 7220-7232.	4.2	20
731	An Energy-Efficient 3D Cross-Ring Accelerator With 3D-SRAM Cubes for Hybrid Deep Neural Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 776-788.	3.6	5
732	Custom Hardware Architectures for Deep Learning on Portable Devices: A Review. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 6068-6088.	11.3	21
733	Energy modeling of Hoeffding tree ensembles. Intelligent Data Analysis, 2021, 25, 81-104.	0.9	4
734	Reliable Test Architecture With Test Cost Reduction for Systolic-Based DNN Accelerators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1537-1541.	3.0	2
735	Collaborative Edge Computing With FPGA-Based CNN Accelerators for Energy-Efficient and Time-Aware Face Tracking System. IEEE Transactions on Computational Social Systems, 2022, 9, 252-266.	4.4	28
736	A Multiplier-Less Convolutional Neural Network Inference Accelerator for Intelligent Edge Devices. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 739-750.	3.6	5
737	Memory-Augmented Neural Networks on FPGA for Real-Time and Energy-Efficient Question Answering. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 162-175.	3.1	2
738	A Raw Image-Based End-to-End Object Detection Accelerator Using HOG Features. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 322-333.	5.4	11
739	Olympus: Reaching Memory-Optimality on DNN Processors. IEEE Transactions on Computers, 2021, , 1-1.	3.4	1
740	DyGA: A Hardware-Efficient Accelerator With Traffic-Aware Dynamic Scheduling for Graph Convolutional Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 5095-5107.	5.4	1
741	ODMDEF: On-Device Multi-DNN Execution Framework Utilizing Adaptive Layer-Allocation on General Purpose Cores and Accelerators. IEEE Access, 2021, 9, 85403-85417.	4.2	6
742	Power-Efficient Deep Convolutional Neural Network Design Through Zero-Gating PEs and Partial-Sum Reuse Centric Dataflow. IEEE Access, 2021, 9, 17411-17420.	4.2	5
743	Hardware-Aware NAS Framework with Layer Adaptive Scheduling on Embedded System. , 2021, , .		2

#	Article	IF	Citations
744	Tile-based Code Generation for Efficiently Accessing to Scratchpad Memory. , 2021, , .		0
745	10T SRAM Computing-in-Memory Macros for Binary and Multibit MAC Operation of DNN Edge Processors. IEEE Access, 2021, 9, 71262-71276.	4.2	12
746	Stealthy and Robust Glitch Injection Attack on Deep Learning Accelerator for Target With Variational Viewpoint. IEEE Transactions on Information Forensics and Security, 2021, 16, 1928-1942.	6.9	5
747	A New Low Power Schema for Stream Processors Front-End with Power-Aware DA-Based FIR Filters by Investigation of Image Transitions Sparsity. Circuits, Systems, and Signal Processing, 2021, 40, 3456-3478.	2.0	0
748	Low-Latency In Situ Image Analytics With FPGA-Based Quantized Convolutional Neural Network. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 2853-2866.	11.3	12
749	ComPreEND: Computation Pruning through Predictive Early Negative Detection for ReLU in a Deep Neural Network Accelerator. IEEE Transactions on Computers, 2022, 71, 1537-1550.	3.4	2
750	Evaluating Spatial Accelerator Architectures with Tiled Matrix-Matrix Multiplication. IEEE Transactions on Parallel and Distributed Systems, 2022, 33, 1002-1014.	5.6	10
751	Real-Time SSDLite Object Detection on FPGA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1192-1205.	3.1	20
752	Minimizing Off-Chip Memory Access for CNN Accelerators. IEEE Consumer Electronics Magazine, 2021, , 1-1.	2.3	1
753	Evaluation Metrics for the Cost of Data Movement in Deep Neural Network Acceleration. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2021, E104.A, 1488-1498.	0.3	0
754	A 7-nm Compute-in-Memory SRAM Macro Supporting Multi-Bit Input, Weight and Output and Achieving 351 TOPS/W and 372.4 GOPS. IEEE Journal of Solid-State Circuits, 2021, 56, 188-198.	5.4	80
755	Rubik: A Hierarchical Architecture for Efficient Graph Neural Network Training. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 936-949.	2.7	21
756	A Review of FPGAâ€Based Custom Computing Architecture for Convolutional Neural Network Inference. Chinese Journal of Electronics, 2021, 30, 1-17.	1.5	9
757	A High-Level Modeling Framework for Estimating Hardware Metrics of CNN Accelerators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4783-4795.	5.4	6
758	Binarized Encoder-Decoder Network and Binarized Deconvolution Engine for Semantic Segmentation. IEEE Access, 2021, 9, 8006-8027.	4.2	5
759	Algorithm-Based Fault Tolerance for Convolutional Neural Networks. IEEE Transactions on Parallel and Distributed Systems, 2021, , 1-1.	5.6	33
760	Energy-Efficient Accelerator Design With Tile-Based Row-Independent Compressed Memory for Sparse Compressed Convolutional Neural Networks. IEEE Open Journal of Circuits and Systems, 2021, 2, 131-143.	1.9	3
761	Improving Efficiency in Neural Network Accelerator using Operands Hamming Distance Optimization. , 2021, , .		0

#	Article	IF	Citations
762	Task Parallelism-Aware Deep Neural Network Scheduling on Multiple Hybrid Memory Cube-Based Processing-in-Memory. IEEE Access, 2021, 9, 68561-68572.	4.2	7
763	Nonconventional Computer Arithmetic Circuits, Systems and Applications. IEEE Circuits and Systems Magazine, 2021, 21, 6-40.	2.3	27
764	Efficient Memory Organization for DNN Hardware Accelerator Implementation on PSoC. Electronics (Switzerland), 2021, 10, 94.	3.1	4
765	C-Testing and Efficient Fault Localization for AI Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2348-2361.	2.7	13
766	Edge Artificial Intelligence Chips for the Cyberphysical Systems Era. Computer, 2021, 54, 84-88.	1.1	10
767	Improving the Accuracy of Spiking Neural Networks for Radar Gesture Recognition Through Preprocessing. IEEE Transactions on Neural Networks and Learning Systems, 2023, 34, 2869-2881.	11.3	10
768	A Survey on Federated Learning for Resource-Constrained IoT Devices. IEEE Internet of Things Journal, 2022, 9, 1-24.	8.7	215
769	CUTIE: Beyond PetaOp/s/W Ternary DNN Inference Acceleration With Better-Than-Binary Energy Efficiency. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1020-1033.	2.7	9
770	FlexScore: Quantifying Flexibility. IEEE Computer Architecture Letters, 2021, 20, 58-4.	1.5	1
771	Evaluation Method of Deep Learning-Based Embedded Systems for Traffic Sign Detection. IEEE Access, 2021, 9, 101217-101238.	4.2	24
772	Search-Free Inference Acceleration for Sparse Convolutional Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2156-2169.	2.7	2
773	Low-Cost Side-Channel Secure Standard 6T-SRAM-Based Memory With a 1% Area and Less Than 5% Latency and Power Overheads. IEEE Access, 2021, 9, 91764-91776.	4.2	2
774	Vau Da Muntanialas: Energy-Efficient Multi-Die Scalable Acceleration of RNN Inference. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 244-257.	5.4	3
775	Hardware-Aware Design for Edge Intelligence. IEEE Open Journal of Circuits and Systems, 2021, 2, 113-127.	1.9	7
776	Customizable Vector Acceleration in Extreme-Edge Computing: A RISC-V Software/Hardware Architecture Study on VGG-16 Implementation. Electronics (Switzerland), 2021, 10, 518.	3.1	5
777	A cross-layer approach towards developing efficient embedded Deep Learning systems. Microprocessors and Microsystems, 2022, 88, 103609.	2.8	6
778	Object Detection Based on Faster R-Cnn. International Journal of Engineering and Advanced Technology, 2021, 10, 72-76.	0.3	4
779	Heterogeneous Mixed-Signal Monolithic 3-D In-Memory Computing Using Resistive RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 386-396.	3.1	18

#	Article	IF	Citations
780	Chasing Carbon: The Elusive Environmental Footprint of Computing. , 2021, , .		28
781	GradPIM: A Practical Processing-in-DRAM Architecture for Gradient Descent. , 2021, , .		15
782	Memory level neural network: A time-varying neural network for memory input processing. Neurocomputing, 2021, 425, 256-265.	5.9	2
783	Modeling and Optimization of SRAM-based In-Memory Computing Hardware Design. , 2021, , .		9
784	An Efficient FIFO Based Accelerator for Convolutional Neural Networks. Journal of Signal Processing Systems, 2021, 93, 1117-1129.	2.1	5
785	High Level Synchronization and Computations of Feed Forward Cut-Set based Multiply Accumulate Unit. Journal of Physics: Conference Series, 2021, 1804, 012201.	0.4	1
786	NP-CGRA: Extending CGRAs for Efficient Processing of Light-weight Deep Neural Networks. , 2021, , .		5
787	A Case for Emerging Memories in DNN Accelerators. , 2021, , .		5
788	S2N2: A FPGA Accelerator for Streaming Spiking Neural Networks. , 2021, , .		28
789	Deep Unfolded Extended Conjugate Gradient Method for Massive MIMO Processing with Application to Reciprocity Calibration. Journal of Signal Processing Systems, 2021, 93, 965-975.	2.1	0
790	Marvel: A Vertical Resistive Accelerator for Low-Power Deep Learning Inference in Monolithic 3D. , 2021, , .		3
791	SNAP: An Efficient Sparse Neural Acceleration Processor for Unstructured Sparse Deep Neural Network Inference. IEEE Journal of Solid-State Circuits, 2021, 56, 636-647.	5.4	34
792	Mixed-Signal Neuromorphic Computing Circuits Using Hybrid CMOS-RRAM Integration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 581-586.	3.0	6
793	A TensorFlow and System Simulator Integration Approach to Estimate Hardware Metrics of Convolution Accelerators. , 2021, , .		1
794	Freely scalable and reconfigurable optical hardware for deep learning. Scientific Reports, 2021, 11, 3144.	3.3	32
795	Neural Synaptic Plasticity-Inspired Computing: A High Computing Efficient Deep Convolutional Neural Network Accelerator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 728-740.	5.4	13
796	OR-ML: Enhancing Reliability for Machine Learning Accelerator with Opportunistic Redundancy. , 2021, , .		1
797	Design of Thermometer Coding and One-Hot Coding. , 2021, , .		3

#	Article	IF	Citations
798	Artificial intelligence enhances the performance of chaotic baseband wireless communication. IET Communications, 2021, 15, 1467-1479.	2.2	7
799	Monolithic 3D Integrated Circuits: Recent Trends and Future Prospects. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 837-843.	3.0	20
800	Rate-Distortion Optimized Coding for Efficient CNN Compression. , 2021, , .		5
801	Klessydra-T: Designing Vector Coprocessors for Multithreaded Edge-Computing Cores. IEEE Micro, 2021, 41, 64-71.	1.8	19
802	Carry-Propagation-Adder-Factored Gemmini Systolic Array for Machine Learning Acceleration. Electronics (Switzerland), 2021, 10, 652.	3.1	4
803	Towards an Efficient CNN Inference Architecture Enabling In-Sensor Processing. Sensors, 2021, 21, 1955.	3.8	9
804	BitSystolic: A 26.7 TOPS/W 2b~8b NPU With Configurable Data Flows for Edge Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1134-1145.	5.4	8
805	A CNN Accelerator with Embedded Risc-V Controllers. , 2021, , .		3
806	Artificial Intelligence Accelerators Based on Graphene Optoelectronic Devices. Advanced Photonics Research, 2021, 2, 2100048.	3.6	11
807	Toward Functional Safety of Systolic Array-Based Deep Learning Hardware Accelerators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 485-498.	3.1	33
809	Editorial: Understanding and Bridging the Gap Between Neuromorphic Computing and Machine Learning. Frontiers in Computational Neuroscience, 2021, 15, 665662.	2.1	9
810	Low Power and Area Efficient Borrow Save Adder for MAC Unit in VLSI Application. Information Technology in Industry, 2021, 9, 828-834.	0.2	0
811	Design and Implementation of Convolutional Neural Network Accelerator Based on RISCV. Journal of Physics: Conference Series, 2021, 1871, 012073.	0.4	1
812	CLU. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-25.	2.3	4
813	HardCompress: A Novel Hardware-based Low-power Compression Scheme for DNN Accelerators. , 2021, , .		3
814	RRAM-DNN: An RRAM and Model-Compression Empowered All-Weights-On-Chip DNN Accelerator. IEEE Journal of Solid-State Circuits, 2021, 56, 1105-1115.	5.4	18
815	AdequateDL: Approximating Deep Learning Accelerators. , 2021, , .		1
816	Dynamic Mapping Mechanism to Compute DNN Models on a Resource-limited NoC Platform. , 2021, , .		1

#	Article	IF	Citations
817	A Survey of Algorithmic and Hardware Optimization Techniques for Vision Convolutional Neural Networks on FPGAs. Neural Processing Letters, 2021, 53, 2331-2377.	3.2	8
818	DiAG: a dataflow-inspired architecture for general-purpose processors. , 2021, , .		5
819	ROMANet: Fine-Grained Reuse-Driven Off-Chip Memory Access Management and Data Organization for Deep Neural Network Accelerators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 702-715.	3.1	19
820	Design Space Optimization of Shared Memory Architecture in Accelerator-rich Systems. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-31.	2.6	4
821	Practically Deploying Heavyweight Adaptive Bitrate Algorithms With Teacher-Student Learning. IEEE/ACM Transactions on Networking, 2021, 29, 723-736.	3.8	11
822	Embedded Intelligence on FPGA: Survey, Applications and Challenges. Electronics (Switzerland), 2021, 10, 895.	3.1	46
823	Neural Network Training With Stochastic Hardware Models and Software Abstractions. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1532-1542.	5.4	7
824	Design of 2D Systolic Array Accelerator for Quantized Convolutional Neural Networks. , 2021, , .		1
825	Adaptable Parallel Acceleration Strategy for Dynamic Monte Carlo Simulations of Polymerization with Microscopic Resolution. Industrial & Engineering Chemistry Research, 2021, 60, 6173-6187.	3.7	5
826	Z-PIM: A Sparsity-Aware Processing-in-Memory Architecture With Fully Variable Weight Bit-Precision for Energy-Efficient Deep Neural Networks. IEEE Journal of Solid-State Circuits, 2021, 56, 1093-1104.	5.4	29
827	A Lightweight Error-Resiliency Mechanism for Deep Neural Networks. , 2021, , .		6
828	Trends and Opportunities for SRAM Based In-Memory and Near-Memory Computation. , 2021, , .		3
829	Architecture, Dataflow and Physical Design Implications of 3D-ICs for DNN-Accelerators. , 2021, , .		3
830	Accelerating Neural Network Inference on FPGA-Based Platformsâ€"A Survey. Electronics (Switzerland), 2021, 10, 1025.	3.1	40
831	Visibility Restoration: A Systematic Review and Meta-Analysis. Sensors, 2021, 21, 2625.	3.8	13
832	Low-Profile Metasurface-Based Diaphragm for Compartment Shielding of Microwave Cavities. IEEE Transactions on Microwave Theory and Techniques, 2021, 69, 2048-2059.	4.6	7
833	An FPGA-Based Hardware Accelerator for CNNs Inference on Board Satellites: Benchmarking with Myriad 2-Based Solution for the CloudScout Case Study. Remote Sensing, 2021, 13, 1518.	4.0	32
834	DF-LNPU: A Pipelined Direct Feedback Alignment-Based Deep Neural Network Learning Processor for Fast Online Learning. IEEE Journal of Solid-State Circuits, 2021, 56, 1630-1640.	5.4	15

#	Article	IF	Citations
835	Quantum Statistical Transport Phenomena in Memristive Computing Architectures. Physical Review Applied, 2021, 15, .	3.8	2
836	Batch Normalization Processor Design for Convolution Neural Network Training and Inference. , 2021, , .		9
837	Low Energy Domain Wall Memory Based Convolution Neural Network Design with Optimizing MAC Architecture. , 2021, , .		1
838	High Utilization Energy-Aware Real-Time Inference Deep Convolutional Neural Network Accelerator. , 2021, , .		5
839	Exploring the Accuracy â€“ Energy Trade-off in Machine Learning. , 2021, , .		16
840	Adaptive Extreme Edge Computing for Wearable Devices. Frontiers in Neuroscience, 2021, 15, 611300.	2.8	67
841	A Computational Efficient Architecture for Extremely Sparse Stereo Network. , 2021, , .		0
842	SWM: A High-Performance Sparse-Winograd Matrix Multiplication CNN Accelerator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 936-949.	3.1	19
843	A survey of in-spin transfer torque MRAM computing. Science China Information Sciences, 2021, 64, 1.	4.3	22
844	A 5.9Î¼W Ultra-Low-Power Dual-Resolution CIS Chip of Sensing-with-Computing for Always-on Intelligent Visual Devices. , 2021, , .		0
845	Comparison of Digit-Serial and Bit-Level Designs for Acceleration of Convolutional Neural Network Computation. , 2021, , .		1
846	Transport Triggered near Memory Accelerator for Deep Learning. , 2021, , .		0
847	Accelerating Convolutional Neural Network Inference Based on a Reconfigurable Sliced Systolic Array. , 2021, , .		4
848	An Optimized Hardware Implementation of Deep Learning Inference for Diabetes Prediction. , 2021, , .		4
849	Design space for scaling-in general purpose computing within the DDR DRAM hierarchy for map-reduce workloads. , 2021, , .		2
850	High Performance Kernel Architecture for Convolutional Neural Network Acceleration. Journal of Circuits, Systems and Computers, 2021, 30, .	1.5	3
851	Mapping and virtual neuron assignment algorithms for MAERI accelerator. Journal of Supercomputing, 0, , 1.	3.6	0
852	sEMG-Based Continuous Estimation of Finger Kinematics via Large-Scale Temporal Convolutional Network. Applied Sciences (Switzerland), 2021, 11, 4678.	2.5	16

#	Article	IF	Citations
853	Deep Neural Network Accelerator Design for the Multi-task, High performance, and Energy-efficient Edge Computing. , 2021, , .		0
854	unzipFPGA: Enhancing FPGA-based CNN Engines with On-the-Fly Weights Generation. , 2021, , .		6
855	Accumulation-Aware Shift and Difference-Add Booth Multiplier for Energy-Efficient Convolutional Neural Network Inference. Circuits, Systems, and Signal Processing, 2021, 40, 6050-6066.	2.0	0
856	Link Bit-Error-Rate Requirement Analysis for Deep Neural Network Accelerators. , 2021, , .		1
857	An Application Specific Vector Processor for CNN-Based Massive MIMO Positioning. , 2021, , .		2
858	ELSA: Hardware-Software Co-design for Efficient, Lightweight Self-Attention Mechanism in Neural Networks. , 2021, , .		40
859	GoSPA: An Energy-efficient High-performance Globally Optimized SParse Convolutional Neural Network Accelerator. , 2021, , .		34
860	2Deep: Enhancing Side-Channel Attacks on Lattice-Based Key-Exchange via 2-D Deep Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1217-1229.	2.7	6
861	Dynamic Regularization on Activation Sparsity for Neural Network Efficiency Improvement. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-16.	2.3	0
862	Reconfigurable Intelligent Surface for Green Edge Inference. IEEE Transactions on Green Communications and Networking, 2021, 5, 964-979.	5.5	36
863	Accelerating DNNs inference with predictive layer fusion. , 2021, , .		4
864	Analyzing the Energy-Latency-Area-Accuracy Trade-off Across Contemporary Neural Networks. , 2021, , .		2
865	Tile-Based Architecture Exploration for Convolutional Accelerators in Deep Neural Networks. , 2021, , .		2
866	NASGuard: A Novel Accelerator Architecture for Robust Neural Architecture Search (NAS) Networks. , 2021, , .		1
867	Sparsity-Aware and Re-configurable NPU Architecture for Samsung Flagship Mobile SoC. , 2021, , .		41
868	STICKER-T: An Energy-Efficient Neural Network Processor Using Block-Circulant Algorithm and Unified Frequency-Domain Acceleration. IEEE Journal of Solid-State Circuits, 2021, 56, 1936-1948.	5.4	6
869	ALPINE. , 2021, , .		0
871	Advancements in Microprocessor Architecture for Ubiquitous Alâ€"An Overview on History, Evolution, and Upcoming Challenges in AI Implementation. Micromachines, 2021, 12, 665.	2.9	11

#	Article	IF	Citations
872	Flexible-width Bit-level Compressor for Convolutional Neural Network. , 2021, , .		2
873	Non-Invasive Air-Writing Using Deep Neural Network. , 2021, , .		1
874	Two Sides of the Same Coin: Boons and Banes of Machine Learning in Hardware Security. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 228-251.	3.6	4
875	Full Custom Layout of Neural Network Processing Element Using Push Pull D Flip Flop and Modified Carry Look Ahead Adder. , 2021, , .		0
876	A New Lightweight In Situ Adversarial Sample Detector for Edge Deep Neural Network. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 252-266.	3.6	4
877	A Simplified CNNs Visual Perception Learning Network Algorithm for Foods Recognition. Computers and Electrical Engineering, 2021, 92, 107152.	4.8	10
878	Computing Utilization Enhancement for Chiplet-based Homogeneous Processing-in-Memory Deep Learning Processors. , 2021, , .		1
879	Are Mobile DNN Accelerators Accelerating DNNs?. , 2021, , .		4
880	CNN-DMA. , 2021, , .		2
881	Albireo: Energy-Efficient Acceleration of Convolutional Neural Networks via Silicon Photonics. , 2021, , .		13
882	Mini Pool: Pooling hardware architecture using minimized local memory for CNN accelerators. , 2021, , .		4
883	Analyzing the Soft Error Reliability of Convolutional Neural Networks on Graphics Processing Unit. Journal of Physics: Conference Series, 2021, 1933, 012045.	0.4	1
884	An FPGA-Based Convolutional Neural Network Coprocessor. Wireless Communications and Mobile Computing, 2021, 2021, 1-12.	1.2	2
885	CAP-RAM: A Charge-Domain In-Memory Computing 6T-SRAM for Accurate and Precision-Programmable CNN Inference. IEEE Journal of Solid-State Circuits, 2021, 56, 1924-1935.	5.4	46
886	Implementation of post processing hardware for real-time object detection in CNN acceleration system. , 2021, , .		2
887	Hardware Dataflow for Convolutional Neural Network Accelerator. , 2021, , .		0
888	High-throughput Near-Memory Processing on CNNs with 3D HBM-like Memory. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-20.	2.6	4
889	An Efficient and Flexible Accelerator Design for Sparse Convolutional Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2936-2949.	5.4	27

#	Article	IF	Citations
891	Case Study on Integrated Architecture for In-Memory and In-Storage Computing. Electronics (Switzerland), 2021, 10, 1750.	3.1	3
892	A Survey of On-Device Machine Learning. ACM Transactions on Internet of Things, 2021, 2, 1-49.	4.6	51
893	Deep Learning in the Industrial Internet of Things: Potentials, Challenges, and Emerging Applications. IEEE Internet of Things Journal, 2021, 8, 11016-11040.	8.7	102
894	3D-aCortex: an ultra-compact energy-efficient neurocomputing platform based on commercial 3D-NAND flash memories. Neuromorphic Computing and Engineering, 2021, 1, 014001.	5.9	13
895	Heterogeneity-Aware Scheduling on SoCs for Autonomous Vehicles. IEEE Computer Architecture Letters, 2021, 20, 82-85.	1.5	6
896	Rethinking Benchmarks for Neuromorphic Learning Algorithms. , 2021, , .		0
897	FPRA: A Fine-grained Parallel RRAM Architecture. , 2021, , .		3
898	Convolver Design and Convolve-Accumulate Unit Design for Low-Power Edge Computing. Sensors, 2021, 21, 5081.	3.8	1
899	Systolic-Array Spiking Neural Accelerators with Dynamic Heterogeneous Voltage Regulation. , 2021, , .		2
900	Colonnade: A Reconfigurable SRAM-Based Digital Bit-Serial Compute-In-Memory Macro for Processing Neural Networks. IEEE Journal of Solid-State Circuits, 2021, 56, 2221-2233.	5.4	62
901	DOSAGE: Generating Domain-Specific Accelerators for Resource-Constrained Computing. , 2021, , .		0
902	DIAN: Differentiable Accelerator-Network Co-Search Towards Maximal DNN Efficiency. , 2021, , .		5
903	A Marr's Threeâ€Level Analytical Framework for Neuromorphic Electronic Systems. Advanced Intelligent Systems, 2021, 3, 2100054.	6.1	3
904	High-efficient MPSoC-based CNNs accelerator with optimized storage and dataflow. Journal of Supercomputing, 2022, 78, 3205-3225.	3.6	0
905	Direct Gradient Calculation: Simple and Variationâ€Tolerant Onâ€Chip Training Method for Neural Networks. Advanced Intelligent Systems, 2021, 3, 2100064.	6.1	3
906	COMPAC: Compressed Time-Domain, Pooling-Aware Convolution CNN Engine With Reduced Data Movement for Energy-Efficient AI Computing. IEEE Journal of Solid-State Circuits, 2021, 56, 2205-2220.	5.4	12
907	NEMO-CNN: An Efficient Near-Memory Accelerator for Convolutional Neural Networks. , 2021, , .		2
908	ZigZag: Enlarging Joint Architecture-Mapping Design Space Exploration for DNN Accelerators. IEEE Transactions on Computers, 2021, 70, 1160-1174.	3.4	58

#	Article	IF	Citations
909	An Energy-Efficient Accelerator for Rain Removal Based on Convolutional Neural Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2957-2961.	3.0	2
910	CARLA: A Convolution Accelerator With a Reconfigurable and Low-Energy Architecture. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3184-3196.	5.4	7
911	Balancing memory-accessing and computing over sparse DNN accelerator via efficient data packaging. Journal of Systems Architecture, 2021, 117, 102094.	4.3	5
912	nZESPA: A Near-3D-Memory Zero Skipping Parallel Accelerator for CNNs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1573-1585.	2.7	2
913	Enabling Design Methodologies and Future Trends for Edge AI: Specialization and Codesign. IEEE Design and Test, 2021, 38, 7-26.	1.2	24
914	Low-Power Ultra-Small Edge AI Accelerators for Image Recognition with Convolution Neural Networks: Analysis and Future Directions. Electronics (Switzerland), 2021, 10, 2048.	3.1	8
915	An Arbitrary Kernel-size Applicable NoC-based DNN Processor Design with Hybrid Data Reuse. , 2021, , .		2
916	An Energy-Efficient Inference Method in Convolutional Neural Networks Based on Dynamic Adjustment of the Pruning Level. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-20.	2.6	1
917	Dynamic Dataflow Scheduling and Computation Mapping Techniques for Efficient Depthwise Separable Convolution Acceleration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3279-3292.	5.4	19
918	Low power and single multiplier design for 2D convolutions. , 2021, , .		0
919	A Multi-Precision Bit-Serial Hardware Accelerator IP for Deep Learning Enabled Internet-of-Things. , 2021, , .		1
920	A Charge-Domain Scalable-Weight In-Memory Computing Macro With Dual-SRAM Architecture for Precision-Scalable DNN Accelerators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3305-3316.	5.4	30
921	SiP-ML. , 2021, , .		26
922	Evaluating the Performance, Energy and Area Tradeoffs of ATHENA in Superscalar Processors. , 2021, , .		0
924	Enabling on-device classification of ECG with compressed learning for health IoT. Microelectronics Journal, 2021, 115, 105188.	2.0	13
925	Evaluating performance of AI operators using roofline model. Applied Intelligence, 0, , 1.	5.3	0
926	Edge computing with optical neural networks via WDM weight broadcasting. , 2021, , .		5
927	An FPGA-Based Energy-Efficient Reconfigurable Convolutional Neural Network Accelerator for Object Recognition Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3143-3147.	3.0	22

#	Article	IF	Citations
928	Similarity-Aware Architecture/Compiler Co-Designed Context-Reduction Framework for Modulo-Scheduled CGRA. Electronics (Switzerland), 2021, 10, 2210.	3.1	2
929	Simplicial computation: A methodology to compute vectorâ€“vector multiplications with reduced complexity. International Journal of Circuit Theory and Applications, 2021, 49, 3766-3788.	2.0	4
930	A Time-Domain Binary CNN Engine With Error-Detection-Based Resilience in 28nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3177-3181.	3.0	3
931	HNPU: An Adaptive DNN Training Processor Utilizing Stochastic Dynamic Fixed-Point and Active Bit-Precision Searching. IEEE Journal of Solid-State Circuits, 2021, 56, 2858-2869.	5.4	36
932	An accurate and fair evaluation methodology for SNN-based inferencing with full-stack hardware design space explorations. Neurocomputing, 2021, 455, 125-138.	5.9	3
933	Neural Network-based Online Fault Diagnosis in Wireless-NoC Systems. Journal of Electronic Testing: Theory and Applications (JETTA), 2021, 37, 545-559.	1.2	3
934	Dadu-Eye: A 5.3 TOPS/W, 30 fps/1080p High Accuracy Stereo Vision Accelerator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4207-4220.	5.4	10
935	A predictor circuit and a delay-aware algorithm for identifying data transfer pattern on NoC-based communication networks. Microelectronics Journal, 2021, 116, 105250.	2.0	2
936	Â±CIM SRAM for Signed In-Memory Broad-Purpose Computing From DSP to Neural Processing. IEEE Journal of Solid-State Circuits, 2021, 56, 2981-2992.	5.4	18
937	Hardware Acceleration of Sparse and Irregular Tensor Computations of ML Models: A Survey and Insights. Proceedings of the IEEE, 2021, 109, 1706-1752.	21.3	35
938	Intermittent-Aware Neural Architecture Search. Transactions on Embedded Computing Systems, 2021, 20, 1-27.	2.9	18
939	Reliability Enhancement of Inverter-Based Memristor Crossbar Neural Networks Using Mathematical Analysis of Circuit Non-Idealities. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4310-4323.	5.4	8
940	TIMAQ: A Time-Domain Computing-in-Memory-Based Processor Using Predictable Decomposed Convolution for Arbitrary Quantized DNNs. IEEE Journal of Solid-State Circuits, 2021, 56, 3021-3038.	5.4	9
941	Single-poly floating-gate memory cell options for analog neural networks. Solid-State Electronics, 2021, 185, 108062.	1.4	0
942	On-chip adaptive matching learning with charge-trap synapse device and ReLU activation circuit. Solid-State Electronics, 2021, 186, 108177.	1.4	5
943	An Elastic Task Scheduling Scheme on Coarse-Grained Reconfigurable Architectures. IEEE Transactions on Parallel and Distributed Systems, 2021, 32, 3066-3080.	5.6	6
944	Configurable Multi-directional Systolic Array Architecture for Convolutional Neural Networks. Transactions on Architecture and Code Optimization, 2021, 18, 1-24.	2.0	12
945	TMA: Teraâ€MACs/W neural hardware inference accelerator with a multiplierâ€less massive parallel processor. International Journal of Circuit Theory and Applications, 2021, 49, 1399-1409.	2.0	4

#	Article	IF	Citations
946	Early-Stage Neural Network Hardware Performance Analysis. Sustainability, 2021, 13, 717.	3.2	13
947	Chip and System Design of Intrinsic Image Decomposition and Enhancement Based on Conditional Generative Adversarial Network. , 2021, , .		0
948	MARS: Multimacro Architecture SRAM CIM-Based Accelerator With Co-Designed Compressed Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1550-1562.	2.7	8
949	A Selective Mitigation Technique of Soft Errors for DNN Models Used in Healthcare Applications: DenseNet201 Case Study. IEEE Access, 2021, 9, 65803-65823.	4.2	16
950	Highly Efficient Test Architecture for Low-Power AI Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2728-2738.	2.7	6
951	Designing Efficient and High-Performance AI Accelerators With Customized STT-MRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1730-1742.	3.1	10
952	A Real-Time Architecture for Pruning the Effectual Computations in Deep Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2030-2041.	5.4	8
953	Minimal Filtering Algorithms for Convolutional Neural Networks. Studies in Computational Intelligence, 2021, , 73-88.	0.9	0
954	Transform Quantization for CNN Compression. IEEE Transactions on Pattern Analysis and Machine Intelligence, 2021, PP, 1-1.	13.9	23
955	S2Engine: A Novel Systolic Architecture for Sparse Convolutional Neural Networks. IEEE Transactions on Computers, 2021, , 1-1.	3.4	10
956	High-Performance Deterministic Stochastic Computing Using Residue Number System. IEEE Design and Test, 2021, 38, 60-68.	1.2	3
957	Row-Streaming Dataflow Using a Chaining Buffer and Systolic Array+ Structure. IEEE Computer Architecture Letters, 2021, 20, 34-37.	1.5	4
958	DeepOpt. , 2021, , .		10
959	Merged Logic and Memory Fabrics for AI Workloads. , 2021, , .		0
960	A Power Efficiency Enhancements of a Multi-Bit Accelerator for Memory Prohibitive Deep Neural Networks. IEEE Open Journal of Circuits and Systems, 2021, 2, 156-169.	1.9	9
961	Energy-efficient deep learning inference on edge devices. Advances in Computers, 2021, 122, 247-301.	1.6	17
962	Early results on deep unfolded conjugate gradientâ€based largeâ€scale MIMO detection. IET Communications, 2021, 15, 435-444.	2.2	2
963	Toward Full-Stack Acceleration of Deep Convolutional Neural Networks on FPGAs. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 3974-3987.	11.3	9

#	Article	IF	Citations
964	S-FLASH: A NAND Flash-based Deep Neural Network Accelerator Exploiting Bit-level Sparsity. IEEE Transactions on Computers, 2021, , 1-1.	3.4	10
965	Design Exploration of ReRAM-Based Crossbar for AI Inference. IEEE Access, 2021, 9, 70430-70442.	4.2	3
966	RSNN: A Software/Hardware Co-Optimized Framework for Sparse Convolutional Neural Networks on FPGAs. IEEE Access, 2021, 9, 949-960.	4.2	19
967	Hybrid Convolution Architecture for Energy-Efficient Deep Neural Network Processing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2017-2029.	5.4	4
968	Silicon Modeling of Spiking Neurons With Diverse Dynamic Behaviors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2199-2212.	2.7	2
969	EFFORT: A Comprehensive Technique to Tackle Timing Violations and Improve Energy Efficiency of Near-Threshold Tensor Processing Units. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1790-1799.	3.1	5
971	A Neural Network Training Processor With 8-Bit Shared Exponent Bias Floating Point and Multiple-Way Fused Multiply-Add Trees. IEEE Journal of Solid-State Circuits, 2022, 57, 965-977.	5.4	14
972	Multiply accumulate operations in memristor crossbar arrays for analog computing. Journal of Semiconductors, 2021, 42, 013104.	3.7	32
973	Learning Without Forgetting: A New Framework for Network Cyber Security Threat Detection. IEEE Access, 2021, 9, 137042-137062.	4.2	7
974	NetAdapt: Platform-Aware Neural Network Adaptation for Mobile Applications. Lecture Notes in Computer Science, 2018, , 289-304.	1.3	228
975	Machine Learning at the Edge. The Frontiers Collection, 2020, , 293-322.	0.2	9
976	Hardware-Aware Softmax Approximation for Deep Neural Networks. Lecture Notes in Computer Science, 2019, , 107-122.	1.3	10
977	Processing Systems for Deep Learning Inference on Edge Devices. Internet of Things, 2020, , 213-240.	1.7	8
978	Deterministic conversion rule for CNNs to efficient spiking convolutional neural networks. Science China Information Sciences, 2020, 63, 1.	4.3	22
979	Industrial process time-series modeling based on adapted receptive field temporal convolution networks concerning multi-region operations. Computers and Chemical Engineering, 2020, 139, 106877.	3.8	12
980	CMOS-integrated memristive non-volatile computing-in-memory for AI edge processors. Nature Electronics, 2019, 2, 420-428.	26.0	161
981	Deep learningâ€based pilotâ€assisted channel state estimator for OFDM systems. IET Communications, 2021, 15, 257-264.	2.2	14
982	Oxide-based filamentary RRAM for deep learning. Journal Physics D: Applied Physics, 2021, 54, 083002.	2.8	20

#	Article	IF	Citations
983	Learning cell for superconducting neural networks. Superconductor Science and Technology, 2021, 34, 015006.	3.5	15
984	Deep Learning Acceleration with Neuron-to-Memory Transformation. , 2020, , .		14
985	Survey of Machine Learning Accelerators. , 2020, , .		74
986	DSIP: A Scalable Inference Accelerator for Convolutional Neural Networks. IEEE Journal of Solid-State Circuits, 2018, 53, 605-618.	5.4	48
987	DUET: Boosting Deep Neural Network Efficiency on Dual-Module Architecture. , 2020, , .		16
988	ComPEND. , 2018, , .		14
989	Scalable-effort ConvNets for multilevel classification. , 2018, , .		8
990	MAERI. ACM SIGPLAN Notices, 2018, 53, 461-475.	0.2	114
991	Google Workloads for Consumer Devices. ACM SIGPLAN Notices, 2018, 53, 316-331.	0.2	30
992	VIBNN. ACM SIGPLAN Notices, 2018, 53, 476-488.	0.2	32
993	QuTiBench. ACM Journal on Emerging Technologies in Computing Systems, 2019, 15, 1-38.	2.3	13
994	AutoDNNchip. , 2020, , .		52
995	What can Machine Learning do for Radio Spectrum Management?. , 2020, , .		4
996	Linear programmable nanophotonic processors. Optica, 2018, 5, 1623.	9.3	240
997	Convolutional Neural Network based for Automatic Text Summarization. International Journal of Advanced Computer Science and Applications, 2019, 10, .	0.7	6
998	Accelerating generalized linear models with MLWeaving. Proceedings of the VLDB Endowment, 2019, 12, 807-821.	3.8	19
999	Deep Learning on Edge. Advances in Computational Intelligence and Robotics Book Series, 2020, , 23-42.	0.4	7
1000	Models of Learning to Classify X-ray Images for the Detection of Pneumonia using Neural Networks. , 2019, , .		36

#	Article	IF	Citations
1008	A TinyML Platform for On-Device Continual Learning With Quantized Latent Replays. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 789-802.	3.6	30
1009	Functionality-Based Processing-in-Memory Accelerator for Deep Convolutional Neural Networks. IEEE Access, 2021, 9, 145098-145108.	4.2	0
1010	M2M: Learning to Enhance Low-Light Image from Model to Mobile FPGA. Lecture Notes in Computer Science, 2021, , 276-287.	1.3	1
1011	An Efficient Deep Learning Accelerator Architecture for Compressed Video Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2808-2820.	2.7	1
1012	NC-Net: Efficient Neuromorphic Computing Using Aggregated Subnets on a Crossbar-Based Architecture With Nonvolatile Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2957-2969.	2.7	6
1013	SMIV: A 16-nm 25-mmÂ² SoC for IoT With Arm Cortex-A53, eFPGA, and Coherent Accelerators. IEEE Journal of Solid-State Circuits, 2022, 57, 639-650.	5.4	6
1014	Signal Integrity and Computing Performance Analysis of a Processing-In-Memory of High Bandwidth Memory (PIM-HBM) Scheme. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 1955-1970.	2.5	10
1015	Secure XOR-CIM Engine: Compute-In-Memory SRAM Architecture With Embedded XOR Encryption. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 2027-2039.	3.1	8
1016	Memory-Efficient CNN Accelerator Based on Interlayer Feature Map Compression. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 668-681.	5.4	11
1017	IECA: An In-Execution Configuration CNN Accelerator With 30.55 GOPS/mmÂ² Area Efficiency. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4672-4685.	5.4	12
1018	An Overview of Sparsity Exploitation in CNNs for On-Device Intelligence With Software-Hardware Cross-Layer Optimizations. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 634-648.	3.6	11
1019	Policy Gradient-Based Core Placement Optimization for Multichip Many-Core Systems. IEEE Transactions on Neural Networks and Learning Systems, 2021, PP, 1-15.	11.3	1
1020	3D Collaborative Judgment MobileNet Based Intelligent Driving System. , 2021, , .		0
1021	Mitigating State-Drift in Memristor Crossbar Arrays for Vector Matrix Multiplication. , 0, , .		2
1022	POMMEL: Exploring Off-Chip Memory Energy & Power Consumption in Convolutional Neural Network Accelerators. , 2021, , .		0
1023	X-Layer: Building Composable Pipelined Dataflows for Low-Rank Convolutions. , 2021, , .		0
1024	PIM-DL: Boosting DNN Inference on Digital Processing In-Memory Architectures via Data Layout Optimizations. , 2021, , .		3
1025	An Accuracy-Improved Fixed-Width Booth Multiplier Enabling Bit-Width Adaptive Truncation Error Compensation. Electronics (Switzerland), 2021, 10, 2511.	3.1	1

#	Article	IF	Citations
1026	Automatic Channel Pruning with Hyper-parameter Search and Dynamic Masking. , 2021, , .		2
1027	RecPipe: Co-designing Models and Hardware to Jointly Optimize Recommendation Quality and Performance. , 2021, , .		13
1028	ENMC: Extreme Near-Memory Classification via Approximate Screening. , 2021, , .		4
1029	High performance accelerators for deep neural networks: A review. Expert Systems, 2022, 39, e12831.	4.5	5
1030	Cohmeleon: Learning-Based Orchestration of Accelerator Coherence in Heterogeneous SoCs. , 2021, , .		10
1031	Distilling Bit-level Sparsity Parallelism for General Purpose Deep Learning Acceleration. , 2021, , .		11
1032	Reducing SRAM Reading Power With Column Data Segment and Weights Correlation Enhancement for CNN Processing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2237-2250.	2.7	1
1033	On the Stability of Analog ReLU Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2426-2430.	2.7	7
1034	Energy-efficient Brainware LSI Based on Stochastic Computation. Ieice Ess Fundamentals Review, 2017, 11, 28-39.	0.1	1
1035	Design of the key Structure of Convolutional Neural Network Reconfigurable Accelerator Based on ASIC. , 2018, , .		1
1036	IP core for efficient zero-run length compression of CNN feature maps. Telfor Journal, 2018, 10, 44-49.	0.7	0
1038	A Convolutional Neural Networks Accelerator Based on Parallel Memory. Communications in Computer and Information Science, 2019, , 160-176.	0.5	0
1039	Deep Fusion: A Software Scheduling Method for Memory Access Optimization. Lecture Notes in Computer Science, 2019, , 277-288.	1.3	3
1040	Latest Advances in Computational Speech Analysis for Mobile Sensing. Studies in Neuroscience, Psychology and Behavioral Economics, 2019, , 141-159.	0.3	2
1041	Multiwavelength Neuromorphic Photonics. , 2019, , .		2
1042	Multiwavelength Neuromorphic Silicon Photonics. , 2019, , .		0
1043	FPGA-Based Emulation of Embedded DRAMs for Statistical Error Resilience Evaluation of Approximate Computing Systems. , 2019, , .		6
1044	USE OF DEEP MACHINE LEARNING METHODS OF ARTIFICIAL NEURAL NETWORKS FOR DESIGNING ALGORITHMS OF ELECTROMYOGRAPHY SIGNAL RECOGNITION IN BIONIC PROSTHESIS. Issues of Radio Electronics, 2019, , 64-75.	0.1	0

#	Article	IF	Citations
1045	CASH. , 2019, , .		5
1046	Digital neuromorphic chips for deep learning inference: a comprehensive study. , 2019, , .		5
1047	Distill-Net. Transactions on Embedded Computing Systems, 2019, 18, 1-20.	2.9	3
1048	A 4-way Matrix Multiply Unit for High Throughput Machine Learning Accelerator. , 2019, , .		2
1049	An energy efficient time-mode digit classification neural network implementation. Philosophical Transactions Series A, Mathematical, Physical, and Engineering Sciences, 2020, 378, 20190163.	3.4	3
1050	Accelerating Inference on Binary Neural Networks with Digital RRAM Processing. IFIP Advances in Information and Communication Technology, 2020, , 257-278.	0.7	1
1051	Dependency-Driven Trace-Based Network-on-Chip Emulation on FPGAs. , 2020, , .		3
1052	Prediction of Tier in Supply Chain Using LSTM and Conv1D-LSTM. Journal of Society of Korea Industrial and Systems Engineering, 2020, 43, 120-125.	0.2	1
1053	BPNet: Branch-pruned Conditional Neural Network for Systematic Time-accuracy Tradeoff. , 2020, , .		4
1054	Error Probability Models for Voltage-Scaled Multiply-Accumulate Units. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1665-1675.	3.1	5
1055	RAMANN. , 2020, , .		10
1056	CLAN: Continuous Learning using Asynchronous Neuroevolution on Commodity Edge Devices. , 2020, , .		1
1057	Dynamic Precision Multiplier For Deep Neural Network Accelerators. , 2020, , .		1
1058	An Inference Accelerator Design for Sparse Convolution Neural Network. , 2021, , .		0
1059	A 1.625 TOPS/W SOC for Deep CNN Training and Inference in 28nm CMOS. , 2021, , .		0
1060	Prospects and applications of photonic neural networks. Advances in Physics: X, 2022, 7, .	4.1	54
1061	Edge Intelligence: Empowering Intelligence to the Edge of Network. Proceedings of the IEEE, 2021, 109, 1778-1837.	21.3	61
1062	DFSNet: Dividing-fuse deep neural networks with searching strategy for distributed DNN architecture. Neurocomputing, 2022, 483, 488-500.	5.9	1

#	Article	IF	Citations
1063	NNBench-X. Transactions on Architecture and Code Optimization, 2020, 17, 1-25.	2.0	2
1064	Floating Point Accuracy Testing in Deep Neural Network Computations via Hypothesis Testing. , 2020, , .		0
1065	Evaluation of On-Chip Accelerator Performance Based on RocketChip. , 2020, , .		3
1066	A multi-purpose visual image processing system based on vision chip. , 2020, , .		0
1067	How Much Does Regularity Help FPGA Placement?. , 2020, , .		2
1068	Huffman Coding Based Encoding Techniques for Fast Distributed Deep Learning. , 2020, , .		4
1069	A Robust Hierarchical Learning Approach for dynamic MEC Networks. , 2020, , .		0
1070	Deep In-Memory Architectures in SRAM: An Analog Approach to Approximate Computing. Proceedings of the IEEE, 2020, 108, 2251-2275.	21.3	24
1071	A 270-mV 6T SRAM Using Row-Based Dual-Phase V_{DD} Control in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4774-4783.	5.4	3
1072	A Ferroelectric-based Volatile/Non-volatile Dual-mode Buffer Memory for Deep Neural Network Accelerators. IEEE Transactions on Computers, 2021, , 1-1.	3.4	2
1073	An Overview of Energy-Efficient Hardware Accelerators for On-Device Deep-Neural-Network Training. IEEE Open Journal of the Solid-State Circuits Society, 2021, 1, 115-128.	2.7	11
1074	A High-Speed NMS Coprocessor for Lightweight Ship Detection Algorithm. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1677-1681.	3.0	6
1075	A Lego-Based Neural Network Design Methodology With Flexible NoC. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 711-724.	3.6	1
1076	ApproxNet: Content and Contention-Aware Video Object Classification System for Embedded Clients. ACM Transactions on Sensor Networks, 2022, 18, 1-27.	3.6	8
1077	Computing Graph Neural Networks: A Survey from Algorithms to Accelerators. ACM Computing Surveys, 2022, 54, 1-38.	23.0	87
1078	The Memory Challenge in Ultra-Low Power Deep Learning. The Frontiers Collection, 2020, , 323-349.	0.2	3
1079	Comprehensive SNN Compression Using ADMM Optimization and Activity Regularization. IEEE Transactions on Neural Networks and Learning Systems, 2023, 34, 2791-2805.	11.3	12
1080	Digital Neural Network Accelerators. The Frontiers Collection, 2020, , 181-202.	0.2	3

#	Article	IF	Citations
1081	Accelerating Sparse Convolutional Neural Networks Based on Dataflow Architecture. Lecture Notes in Computer Science, 2020, , 14-31.	1.3	1
1083	Computational Intelligence in Energy Generation. Advances in Civil and Industrial Engineering Book Series, 2020, , 1-62.	0.2	0
1084	Cross-layer CNN Approximations for Hardware Implementation. Lecture Notes in Computer Science, 2020, , 151-165.	1.3	0
1085	CTA: A Critical Task Aware Scheduling Mechanism for Dataflow Architecture. Lecture Notes in Computer Science, 2020, , 61-77.	1.3	0
1086	A Dynamically Reconfigurable Accelerator Design Using a Sparse-Winograd Decomposition Algorithm for CNNs. Computers, Materials and Continua, 2020, 66, 517-535.	1.9	1
1087	An Automatic-Addressing Architecture With Fully Serialized Access in Racetrack Memory for Energy-Efficient CNNs. IEEE Transactions on Computers, 2022, 71, 235-250.	3.4	5
1089	Designing Efficient Shortcut Architecture for Improving the Accuracy of Fully Quantized Neural Networks Accelerator. , 2020, , .		2
1090	IKW: Inter-Kernel Weights for Power Efficient Edge Computing. IEEE Access, 2020, 8, 90450-90464.	4.2	3
1091	Real-Time Implementation of Artificial Neural Network in FPGA Platform. Advances in Intelligent Systems and Computing, 2020, , 3-13.	0.6	1
1092	CNN-SIM: A Detailed Arquitectural Simulator of CNN Accelerators. Lecture Notes in Computer Science, 2020, , 720-724.	1.3	0
1093	Specializing CGRAs for Light-Weight Convolutional Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3387-3399.	2.7	5
1094	DNNGuard: An Elastic Heterogeneous DNN Accelerator Architecture against Adversarial Attacks. , 2020, , .		18
1095	Meramalnet: A Deep Learning Convolutional Neural Network for Bioactivity Prediction in Structure-based Drug Discovery. , 2020, , .		1
1096	Bringing AI to edge: From deep learningâ€™s perspective. Neurocomputing, 2022, 485, 297-320.	5.9	44
1097	In-memory computing with emerging nonvolatile memory devices. Science China Information Sciences, 2021, 64, 1.	4.3	31
1098	UPTPU: Improving Energy Efficiency of a Tensor Processing Unit through Underutilization Based Power-Gating. , 2021, , .		2
1099	GNNerator: A Hardware/Software Framework for Accelerating Graph Neural Networks. , 2021, , .		10
1101	O-2A: Low Overhead DNN Compression with Outlier-Aware Approximation. , 2020, , .		1

#	Article	IF	Citations
1102	An Efficient Deep Learning Accelerator for Compressed Video Analysis. , 2020, , .		3
1103	Replica Bit-Line Technique for Internal Refresh in Logic-Compatible Gain-Cell Embedded DRAM. Microelectronics Journal, 2020, 101, 104781.	2.0	2
1104	ESNreram: An Energy-Efficient Sparse Neural Network Based on Resistive Random-Access Memory. , 2020, , .		0
1105	Transmuter. , 2020, , .		13
1106	Mixed-Signal Charge-Domain Acceleration of Deep Neural Networks through Interleaved Bit-Partitioned Arithmetic. , 2020, , .		10
1107	Dataflow and microarchitecture coâ€optimisation for sparse CNN on distributed processing element accelerator. IET Circuits, Devices and Systems, 2020, 14, 1185-1194.	1.4	1
1108	A many-core accelerator design for on-chip deep reinforcement learning. , 2020, , .		5
1109	NeuroMAX. , 2020, , .		5
1110	MobiLatice. , 2020, , .		7
1111	XOR-CIM. , 2020, , .		13
1112	A Research and Design of Lightweight Convolutional Neural Networks Accelerator Based on Systolic Array Structure. , 2020, , .		0
1113	Heterogeneous Systolic Array Architecture for Compact CNNs Hardware Accelerators. IEEE Transactions on Parallel and Distributed Systems, 2021, , 1-1.	5.6	3
1114	Quantization of Deep Neural Network Models Considering Per-Layer Computation Complexity for Efficient Execution in Multi-Precision Accelerators. , 2021, , .		0
1115	Reconfigurable Deep Learning Accelerator Hardware Architecture Design for Sparse CNN. , 2021, , .		1
1116	Error Correctable Range-Addressable Lookup for Activation and Quantization in AI Automotive Electronics. , 2021, , .		1
1117	Block-Based Compression for Reducing Indexing Cost of DNN Accelerators. , 2021, , .		0
1118	Knee Lift Detection using Convolutional Neural Network Method with FPGA Hardware Design. , 2021, , .		0
1119	A Survey: Handling Irregularities in Neural Network Acceleration with FPGAs. , 2021, , .		7

#	Article	IF	Citations
1120	AI Accelerator Survey and Trends. , 2021, , .		46
1121	Discussion on the Practice of Neural Network Technology in College Music Teaching. , 2021, , .		0
1122	Evaluation System of Tourism Psychology Teaching Quality Based on Convolutional Neural Network. , 2021, , .		0
1123	Exploration and Generation of Efficient FPGA-based Deep Neural Network Accelerators. , 2021, , .		3
1124	Efficient Fault-Criticality Analysis for AI Accelerators using a Neural Twin. , 2021, , .		7
1125	LOCAL: Low-Complex Mapping Algorithm for Spatial DNN Accelerators. , 2021, , .		2
1126	Exploration of Energy-Efficient Architecture for Graph-Based Point-Cloud Deep Learning. , 2021, , .		1
1127	Tiled Squeeze-and-Excite: Channel Attention With Local Spatial Context. , 2021, , .		5
1128	A High-Efficient and Configurable Hardware Accelerator for Convolutional Neural Network. , 2021, , .		2
1129	Block-Based Compression and Corresponding Hardware Circuits for Sparse Activations. Sensors, 2021, 21, 7468.	3.8	2
1130	An Efficient Dataflow Mapping Method for Convolutional Neural Networks. Neural Processing Letters, 0, , .	3.2	0
1131	A Reconfigurable Posit Tensor Unit with Variable-Precision Arithmetic and Automatic Data Streaming. Journal of Signal Processing Systems, 2021, 93, 1365-1385.	2.1	2
1132	Sparse convolutional neural network acceleration with lossless input feature map compression for resourceâ€constrained systems. IET Computers and Digital Techniques, 2022, 16, 29-43.	1.2	6
1133	A Real-Time FPGA Accelerator Based on Winograd Algorithm for Underwater Object Detection. Electronics (Switzerland), 2021, 10, 2889.	3.1	3
1134	Research on Public Environmental Perception of Emotion, Taking Haze as an Example. International Journal of Environmental Research and Public Health, 2021, 18, 12115.	2.6	1
1135	HiMap: Fast and Scalable High-Quality Mapping on CGRA via Hierarchical Abstraction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3290-3303.	2.7	7
1136	Fast and Low-Power Quantized Fixed Posit High-Accuracy DNN Implementation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 108-111.	3.1	5
1137	Cyclic Sparsely Connected Architectures: From foundations to applications. IEEE Solid-State Circuits Magazine, 2021, 13, 64-76.	0.4	0

#	Article	IF	Citations
1138	STT-BSNN: An In-Memory Deep Binary Spiking Neural Network Based on STT-MRAM. IEEE Access, 2021, 9, 151373-151385.	4.2	12
1139	Hardware/Software Co-design for Convolutional Neural Networks Acceleration: A Survey and Open Issues. Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering, 2021, , 164-178.	0.3	2
1140	FPGA-Based Implementation of an Event-Driven Spiking Multi-Kernel Convolution Architecture. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1682-1686.	3.0	1
1141	Machine Learning for Security in Vehicular Networks: A Comprehensive Survey. IEEE Communications Surveys and Tutorials, 2022, 24, 346-379.	39.4	28
1142	Holistic Network Virtualization and Pervasive Network Intelligence for 6G. IEEE Communications Surveys and Tutorials, 2022, 24, 1-30.	39.4	124
1143	Morphling: A Reconfigurable Architecture for Tensor Computation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4733-4746.	2.7	1
1144	Neural Architecture Search and Hardware Accelerator Co-Search: A Survey. IEEE Access, 2021, 9, 151337-151362.	4.2	19
1145	GCONV Chain: Optimizing the Whole-Life Cost in End-to-end CNN Acceleration. IEEE Transactions on Computers, 2022, 71, 2300-2312.	3.4	2
1146	In Search of the Performance- and Energy-Efficient CNN Accelerators. IEICE Transactions on Electronics, 2021, , .	0.6	0
1147	The Design of Efficient Data Flow and Low-Complexity Architecture for the Configurable Cnn Accelerator. SSRN Electronic Journal, 0, , .	0.4	0
1148	Dandelion: Boosting DNN Usability Under Dataset Scarcity. IEEE Transactions on Computers, 2022, 71, 2487-2498.	3.4	0
1149	Leakage Reuse for Energy Efficient Near-Memory Computing of Heterogeneous DNN Accelerators. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 762-775.	3.6	1
1150	Sparse-PE: A Performance-Efficient Processing Engine Core for Sparse Convolutional Neural Networks. IEEE Access, 2021, 9, 151458-151475.	4.2	6
1151	DeepNVM++: Cross-Layer Modeling and Optimization Framework of Nonvolatile Memories for Deep Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3426-3437.	2.7	8
1153	Scalable and Programmable Neural Network Inference Accelerator Based on In-Memory Computing. IEEE Journal of Solid-State Circuits, 2022, 57, 198-211.	5.4	18
1154	New paradigm of FPGA-based computational intelligence from surveying the implementation of DNN accelerators. Design Automation for Embedded Systems, 2022, 26, 1-27.	1.0	5
1155	Marvel: A Data-Centric Approach for Mapping Deep Learning Operators on Spatial Accelerators. Transactions on Architecture and Code Optimization, 2022, 19, 1-26.	2.0	9
1156	A framework for designing power-efficient inference accelerators in tree-based learning applications. Engineering Applications of Artificial Intelligence, 2022, 109, 104638.	8.1	5

#	Article	IF	Citations
1157	Hybrid Stochastic Computing Circuits in Continuous Statistics Domain. , 2020, , .		0
1158	Scalable Data Generation for Evaluating Mixed-Precision Solvers. , 2020, , .		0
1159	Discrete Integrated Circuit Electronics (DICE). , 2020, , .		2
1160	A DBN Hardware Accelerator for Auditory Scene Classification. , 2020, , .		0
1161	Heterogeneous Edge CNN Hardware Accelerator. , 2020, , .		2
1162	MEISSA: Multiplying Matrices Efficiently in a Scalable Systolic Architecture. , 2020, , .		9
1163	A Reconfigurable DNN Training Accelerator on FPGA. , 2020, , .		2
1164	Towards real-time and real-life image classification and detection using CNN: a review of practical applications requirements, algorithms, hardware and current trends. , 2020, , .		1
1165	Implementation of a Round Robin Processing Element for Deep Learning Accelerator. , 2020, , .		1
1166	Reconfigurable Hardware Architecture Design and Implementation for AI Deep Learning Accelerator. , 2020, , .		5
1167	Dynamic Homeostatic Regulation in Energy-Efficient Time-Locked Neuromorphic Systems. , 2020, , .		0
1168	A Comprehensive Review of ML-based Time-Series and Signal Processing Techniques and their Hardware Implementations. , 2020, , .		3
1169	Exploring Direct Convolution Performance on the Gemmini Accelerator. , 0, , .		2
1170	Area and Energy Efficient 2D Max-Pooling For Convolutional Neural Network Hardware Accelerator. , 2020, , .		8
1171	Fast-BCNN: Massive Neuron Skipping in Bayesian Convolutional Neural Networks. , 2020, , .		11
1172	TensorDash: Exploiting Sparsity to Accelerate Deep Neural Network Training. , 2020, , .		38
1173	Distilling Location Proposals of Unknown Objects through Gaze Information for Human-Robot Interaction. , 2020, , .		7
1174	Booth Fusion: Efficient Bit Fusion Multiplier with Booth Encoding. , 2020, , .		1

#	Article	IF	Citations
1175	High Efficient Bandwidth Utilization Hardware Design and Implement for AI Deep Learning Accelerator. , 2020, , .		2
1176	FullReuse: A Novel ReRAM-based CNN Accelerator Reusing Data in Multiple Levels. , 2020, , .		2
1177	A High-speed Low-cost CNN Inference Accelerator for Depthwise Separable Convolution. , 2020, , .		8
1178	Functional Criticality Classification of Structural Faults in AI Accelerators. , 2020, , .		11
1179	Accelerating Sparse DNN Models without Hardware-Support via Tile-Wise Sparsity. , 2020, , .		23
1180	C-Testing of AI Accelerators. , 2020, , .		9
1181	Block-LMS and RLS adaptive filters using in-memory architectures. , 2020, , .		0
1182	QDRelu: An Activation Function Based On Quantum-Dot Spin-VCSELs. , 2020, , .		1
1183	An Energy-Efficient Deep Neural Network Accelerator Design. , 2020, , .		1
1184	Confidential Machine Learning Computation in Untrusted Environments: A Systems Security Perspective. IEEE Access, 2021, 9, 168656-168677.	4.2	4
1185	A 1.625 TOPS/W SOC for Deep CNN Training and Inference in 28nm CMOS. , 2021, , .		0
1186	Real-Time Hamilton-Jacobi Reachability Analysis of Autonomous System With An FPGA. , 2021, , .		2
1187	Vectorized Winogradâ€™s algorithm for Convolution Neural networks. , 2021, , .		1
1188	Energy-Efficient Deep Neural Networks Implementation on a Scalable Heterogeneous FPGA Cluster. , 2021, , .		0
1189	RISC-VTF: RISC-V Based Extended Instruction Set for Transformer. , 2021, , .		3
1190	A Review of 3D-Dynamic Random-Access Memory based Near-Memory Computation. , 2021, , .		2
1191	WiNN: Wireless Interconnect based Neural Network Accelerator. , 2021, , .		2
1192	Reconfigurable Neural Synaptic Plasticity-Based Stochastic Deep Neural Network Computing. , 2021, , .		0

#	Article	IF	Citations
1193	A Cross-Disciplinary View of Industrial Electronics: Change, Chance, and Challenge. , 2021, , .		1
1194	Simulators for Deep Neural Network Accelerator Design and Analysis: A Brief Review. , 2021, , .		0
1195	Sparsity-aware Power Gating for Tensor Cores. , 2021, , .		3
1196	RAODAT: An Energy-Efficient Reconfigurable AI-based Object Detection and Tracking Processor with Online Learning. , 2021, , .		4
1197	Data Rearrange Unit for Efficient Data Computation in Embedded Systems. , 2021, , .		0
1198	Evolving Complementary Sparsity Patterns for Hardware-Friendly Inference of Sparse DNNs. , 2021, , .		2
1199	STONNE: Enabling Cycle-Level Microarchitectural Simulation for DNN Inference Accelerators. , 2021, , .		11
1200	Improving the accuracy and robustness of RRAM-based in-memory computing against RRAM hardware noise and adversarial attacks. Semiconductor Science and Technology, 2022, 37, 034001.	2.0	6
1201	Pulse coding off-chip learning algorithm for memristive artificial neural network. Chinese Physics B, 2022, 31, 078702.	1.4	1
1202	Designing Novel AAD Pooling in Hardware for a Convolutional Neural Network Accelerator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 303-314.	3.1	23
1203	BEOL-Compatible Superlattice FEFET Analog Synapse With Improved Linearity and Symmetry of Weight Update. IEEE Transactions on Electron Devices, 2022, 69, 2094-2100.	3.0	22
1204	The Data Flow and Architectural Optimizations for a Highly Efficient CNN Accelerator Based on the Depthwise Separable Convolution. Circuits, Systems, and Signal Processing, 2022, 41, 3547-3569.	2.0	3
1205	Towards edge computing in intelligent manufacturing: Past, present and future. Journal of Manufacturing Systems, 2022, 62, 588-611.	13.9	60
1206	Harnessing optoelectronic noises in a photonic generative network. Science Advances, 2022, 8, eabm2956.	10.3	24
1207	AHAR: Adaptive CNN for Energy-Efficient Human Activity Recognition in Low-Power Edge Devices. IEEE Internet of Things Journal, 2022, 9, 13041-13051.	8.7	44
1208	Variation-Tolerant Capacitive Array for Binarized Neural Network. IEEE Electron Device Letters, 2022, 43, 478-481.	3.9	2
1209	Hardware Platform-Aware Binarized Neural Network Model Optimization. Applied Sciences (Switzerland), 2022, 12, 1296.	2.5	1
1210	BitCluster: Fine-Grained Weight Quantization for Load-Balanced Bit-Serial Neural Network Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4747-4757.	2.7	1

#	Article	IF	Citations
1211	Spatial Data Dependence Graph Based Pre-RTL Simulator for Convolutional Neural Network Dataflows. IEEE Access, 2022, 10, 11382-11403.	4.2	1
1212	Low Complexity Joint Impairment Mitigation of I/Q Modulator and PA Using Neural Networks. IEEE Journal on Selected Areas in Communications, 2022, 40, 54-64.	14.0	10
1213	Versa: A 36-Core Systolic Multiprocessor With Dynamically Reconfigurable Interconnect and Memory. IEEE Journal of Solid-State Circuits, 2022, 57, 986-998.	5.4	4
1214	BitBlade: Energy-Efficient Variable Bit-Precision Hardware Accelerator for Quantized Neural Networks. IEEE Journal of Solid-State Circuits, 2022, 57, 1924-1935.	5.4	11
1215	On-Orbit Real-Time Variational Image Destriping: FPGA Architecture and Implementation. IEEE Transactions on Geoscience and Remote Sensing, 2022, 60, 1-12.	6.3	3
1216	DFSynthesizer: Dataflow-based Synthesis of Spiking Neural Networks to Neuromorphic Hardware. Transactions on Embedded Computing Systems, 2022, 21, 1-35.	2.9	10
1217	A Survey of Near-Data Processing Architectures for Neural Networks. Machine Learning and Knowledge Extraction, 2022, 4, 66-102.	5.0	2
1219	Design and Scaffolded Training of an Efficient DNN Operator for Computer Vision on the Edge. Transactions on Embedded Computing Systems, 0, , .	2.9	0
1220	MCPS: a mapping method for MAERI accelerator base on Cartesian Product based Convolution for DNN layers with sparse input feature map. Cluster Computing, 0, , 1.	5.0	0
1221	Review of ASIC accelerators for deep neural network. Microprocessors and Microsystems, 2022, 89, 104441.	2.8	25
1222	EAIS: Energy-aware adaptive scheduling for CNN inference on high-performance GPUs. Future Generation Computer Systems, 2022, 130, 253-268.	7.5	14
1223	Hardware Acceleration of a Generalized Fast 2-D Convolution Method for Deep Neural Networks. IEEE Access, 2022, 10, 16843-16858.	4.2	7
1224	ETA: An Efficient Training Accelerator for DNNs Based on Hardware-Algorithm Co-Optimization. IEEE Transactions on Neural Networks and Learning Systems, 2023, 34, 7660-7674.	11.3	8
1225	MLogNet: A Logarithmic Quantization-Based Accelerator for Depthwise Separable Convolution. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 5220-5231.	2.7	2
1226	An efficient hardware architecture based on an ensemble of deep learning models for COVID -19 prediction. Sustainable Cities and Society, 2022, 80, 103713.	10.4	9
1227	Sextans: A Streaming Accelerator for General-Purpose Sparse-Matrix Dense-Matrix Multiplication. , 2022, , .		24
1228	Nebula: A Scalable and Flexible Accelerator for DNN Multi-Branch Blocks on Embedded Systems. Electronics (Switzerland), 2022, 11, 505.	3.1	2
1229	A low-power, high-accuracy with fully on-chip ternary weight hardware architecture for Deep Spiking Neural Networks. Microprocessors and Microsystems, 2022, 90, 104458.	2.8	4

#	Article	IF	Citations
1230	A Survey on the Optimization of Neural Network Accelerators for Micro-AI On-Device Inference. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 532-547.	3.6	20
1231	Deep Neural Network: An Alternative to Traditional Channel Estimators in Massive MIMO Systems. IEEE Transactions on Cognitive Communications and Networking, 2022, 8, 657-671.	7.9	7
1232	Optimization of Multi-Core Accelerator Performance Based on Accurate Performance Estimation. IEEE Access, 2022, 10, 19629-19642.	4.2	2
1233	STICKER-IM: A 65 nm Computing-in-Memory NN Processor Using Block-Wise Sparsity Optimization and Inter/Intra-Macro Data Reuse. IEEE Journal of Solid-State Circuits, 2022, 57, 2560-2573.	5.4	17
1234	A Real-Time 1280 Ã— 720 Object Detection Chip With 585 MB/s Memory Traffic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 816-825.	3.1	2
1235	Energy-Efficient High-Speed ASIC Implementation of Convolutional Neural Network Using Novel Reduced Critical-Path Design. IEEE Access, 2022, 10, 34032-34045.	4.2	3
1236	SOT-MRAM Digital PIM Architecture With Extended Parallelism in Matrix Multiplication. IEEE Transactions on Computers, 2022, 71, 2816-2828.	3.4	8
1237	PredStereo: An Accurate Real-time Stereo Vision System. , 2022, , .		1
1238	A Deep Learning Accelerator Based on a Streaming Architecture for Binary Neural Networks. IEEE Access, 2022, 10, 21141-21159.	4.2	9
1240	Design of Intra Cluster Access Structure for Distributed Caches of Array Processor. , 2022, , .		0
1241	AINNS: All-Inclusive Neural Network Scheduling Via Accelerator Formalization. IEEE Transactions on Computers, 2023, 72, 559-571.	3.4	0
1242	Functional Criticality Analysis of Structural Faults in AI Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 5657-5670.	2.7	5
1243	CASSANN-v2: A high-performance CNN accelerator architecture with on-chip memory self-adaptive tuning. IEICE Electronics Express, 2022, 19, 20220124-20220124.	0.8	7
1244	Bioâ€Inspired 3D Artificial Neuromorphic Circuits. Advanced Functional Materials, 2022, 32, .	14.9	45
1245	Taurus: a data plane architecture for per-packet ML. , 2022, , .		19
1246	An ultra-compact leaky integrate-and-fire neuron with long and tunable time constant utilizing pseudo resistors for spiking neural networks. Japanese Journal of Applied Physics, 2022, 61, SC1051.	1.5	4
1247	Client-optimized algorithms and acceleration for encrypted compute offloading. , 2022, , .		8
1248	Simulating Neural Network Processors. Wireless Communications and Mobile Computing, 2022, 2022, 1-12.	1.2	0

#	Article	IF	Citations
1249	Intelligent Sensing: Enabling the Next â€œAutomation Ageâ€• , 2022, , .		1
1250	Customizable FPGA-Based Hardware Accelerator for Standard Convolution Processes Empowered with Quantization Applied to LiDAR Data. Sensors, 2022, 22, 2184.	3.8	7
1251	A Survey of Deep Learning on Mobile Devices: Applications, Optimizations, Challenges, and Research Opportunities. Proceedings of the IEEE, 2022, 110, 334-354.	21.3	19
1252	A Survey on Efficient Convolutional Neural Networks and Hardware Acceleration. Electronics (Switzerland), 2022, 11, 945.	3.1	62
1253	A Construction Kit for Efficient Low Power Neural Network Accelerator Designs. Transactions on Embedded Computing Systems, 2022, 21, 1-36.	2.9	0
1254	MobileNets Can Be Lossily Compressed: Neural Network Compression for Embedded Accelerators. Electronics (Switzerland), 2022, 11, 858.	3.1	3
1255	Hardware Demonstration of SRDP Neuromorphic Computing with Online Unsupervised Learning Based on Memristor Synapses. Micromachines, 2022, 13, 433.	2.9	9
1256	Non-fragile l₂-l_{âˆž} state estimation for time-delayed artificial neural networks: an adaptive event-triggered approach. International Journal of Systems Science, 2022, 53, 2247-2259.	5.5	51
1257	RT-RCG: Neural Network and Accelerator Search Towards Effective and Real-time ECG Reconstruction from Intracardiac Electrograms. ACM Journal on Emerging Technologies in Computing Systems, 2022, 18, 1-25.	2.3	1
1258	Compression of Deep Neural Networks based on quantized tensor decomposition to implement on reconfigurable hardware platforms. Neural Networks, 2022, 150, 350-363.	5.9	7
1259	A Convolutional Neural Network on Chip Design Methodology for CNN Hardware Implementation. , 2021, , .		0
1260	Design and Optimization of a Pruning-Efficient DCNN Inference Accelerator. , 2021, , .		0
1261	FLECSim-SoC: A Flexible End-to-End Co-Design Simulation Framework for System on Chips. , 2021, , .		3
1262	Towards Memory-Efficient Neural Networks via Multi-Level in situ Generation. , 2021, , .		1
1263	Multiplier with Reduced Activities and Minimized Interconnect for Inner Product Arrays. , 2021, , .		2
1264	O-HAS: Optical Hardware Accelerator Search for Boosting Both Acceleration Performance and Development Speed. , 2021, , .		5
1265	Sparsity-enhanced Convolutional Neural Network for IoT Cyberattacks Detection. , 2021, , .		0
1266	Performance Evaluation of Systolic DCNN Accelerators. , 2021, , .		0

#	Article	IF	Citations
1267	Stealing Neural Network Models through the Scan Chain: A New Threat for ML Hardware. , 2021, , .		3
1268	A Column Streaming-Based Convolution Engine and Mapping Algorithm for CNN-based Edge AI Accelerators. , 2021, , .		2
1269	Early Prediction of DNN Activation Using Hierarchical Computations. Mathematics, 2021, 9, 3130.	2.2	0
1270	A Highly Efficient Layout-Aware FPGA Overlay Accelerator Mapping Method. , 2021, , .		0
1271	Turbo Detection Aided Autoencoder for Multicarrier Wireless Systems: Integrating Deep Learning Into Channel Coded Systems. IEEE Transactions on Cognitive Communications and Networking, 2022, 8, 600-614.	7.9	7
1272	Structured Term Pruning for Computational Efficient Neural Networks Inference. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 190-203.	2.7	2
1273	Deep Neural Networks-Based Weight Approximation and Computation Reuse for 2-D Image Classification. IEEE Access, 2022, 10, 41551-41563.	4.2	2
1274	A 40-nm MLC-RRAM Compute-in-Memory Macro With Sparsity Control, On-Chip Write-Verify, and Temperature-Independent ADC References. IEEE Journal of Solid-State Circuits, 2022, 57, 2868-2877.	5.4	21
1275	Meta-Modeling for Autoencoder-Based End-to-End Communications Systems. , 2022, , .		1
1276	LINAC: A Spatially Linear Accelerator for Convolutional Neural Networks. IEEE Computer Architecture Letters, 2022, 21, 29-32.	1.5	0
1277	A survey of architectures of neural network accelerators. Scientia Sinica Informationis, 2022, 52, 596.	0.4	0
1278	Minimizing Global Buffer Access in a Deep Learning Accelerator Using a Local Register File with a Rearranged Computational Sequence. Sensors, 2022, 22, 3095.	3.8	1
1279	Applications and Techniques for Fast Machine Learning in Science. Frontiers in Big Data, 2022, 5, 787421.	2.9	20
1280	MONETA: A Processing-In-Memory-Based Hardware Platform for the Hybrid Convolutional Spiking Neural Network With Online Learning. Frontiers in Neuroscience, 2022, 16, 775457.	2.8	3
1281	Efficient Hardware Design and Implementation of the Voting Scheme-Based Convolution. Sensors, 2022, 22, 2943.	3.8	3
1282	Neural Architecture Search Survey: A Hardware Perspective. ACM Computing Surveys, 2023, 55, 1-36.	23.0	15
1285	Accelerating Inference of Convolutional Neural Networks Using In-memory Computing. Frontiers in Computational Neuroscience, 2021, 15, 674154.	2.1	16
1286	RASHT: A Partially Reconfigurable Architecture for Efficient Implementation of CNNs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 860-868.	3.1	4

#	Article	IF	Citations
1287	An SRAM-Based Hybrid Computation-in-Memory Macro Using Current-Reused Differential CCO. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 536-546.	3.6	4
1288	Hybrid Accumulator Factored Systolic Array for Machine Learning Acceleration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 881-892.	3.1	9
1289	Energy-Efficient CNN Personalized Training by Adaptive Data Reformation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 332-336.	2.7	1
1290	Exploiting Wireless Technology for Energy-Efficient Accelerators With Multiple Dataflows and Precision. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2742-2755.	5.4	2
1291	Emerging Energy-Efficient Biosignal-Dedicated Circuit Techniques: A Tutorial Brief. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2592-2597.	3.0	4
1292	Configurable Deep Learning Accelerator with Bitwise-accurate Training and Verification. , 2022, , .		0
1293	Efficient Segment-wise Pruning for DCNN Inference Accelerators. , 2022, , .		0
1294	Establishment of Performance Evaluation Model of Highway Environmental Protection Based on Deep Learning. Wireless Communications and Mobile Computing, 2022, 2022, 1-11.	1.2	0
1295	A Scalable and Adaptive Convolutional Neural Network Accelerator. , 2022, , .		0
1296	An Accelerator for Sparse Convolutional Neural Networks Leveraging Systolic General Matrix-matrix Multiplication. Transactions on Architecture and Code Optimization, 2022, 19, 1-26.	2.0	9
1297	Rate Coding Or Direct Coding: Which One Is Better For Accurate, Robust, And Energy-Efficient Spiking Neural Networks?. , 2022, , .		17
1298	High-performance Reconfigurable DNN Accelerator on a Bandwidth-limited Embedded System. Transactions on Embedded Computing Systems, 2023, 22, 1-20.	2.9	4
1299	Hardware-software co-exploration with racetrack memory based in-memory computing for CNN inference in embedded systems. Journal of Systems Architecture, 2022, , 102507.	4.3	2
1300	Gated-CNN: Combating NBTI and HCI aging effects in on-chip activation memories of Convolutional Neural Network accelerators. Journal of Systems Architecture, 2022, 128, 102553.	4.3	1
1301	Neural Network Training With Asymmetric Crosspoint Elements. Frontiers in Artificial Intelligence, 2022, 5, .	3.4	9
1302	A Fully Integrated Systemâ€onâ€Chip Design with Scalable Resistive Randomâ€Access Memory Tile Design for Analog inâ€Memory Computing. Advanced Intelligent Systems, 2022, 4, .	6.1	5
1303	PYXIS: An Open-Source Performance Dataset Of Sparse Accelerators. , 2022, , .		0
1305	DiVIT: Algorithm and architecture co-design of differential attention in vision transformer. Journal of Systems Architecture, 2022, 128, 102520.	4.3	2

#	Article	IF	Citations
1306	Cain: Automatic Code Generation forÂSimultaneous Convolutional Kernels onÂFocal-plane Sensor-processors. Lecture Notes in Computer Science, 2022, , 181-197.	1.3	7
1307	A Heterogeneous In-Memory Computing Cluster for Flexible End-to-End Inference of Real-World Deep Neural Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 422-435.	3.6	18
1308	Parallel Time Batching: Systolic-Array Acceleration of Sparse Spiking Neural Computation. , 2022, , .		5
1309	The Specialized High-Performance Network on Anton 3. , 2022, , .		3
1310	uSystolic: Byte-Crawling Unary Systolic Array. , 2022, , .		8
1311	MAGMA: An Optimization Framework for Mapping Multiple DNNs on Multiple Accelerator Cores. , 2022, , .		17
1312	Compiler-Driven Simulation of Reconfigurable Hardware Accelerators. , 2022, , .		1
1313	LISA: Graph Neural Network based Portable Mapping on Spatial Accelerators. , 2022, , .		13
1314	Deep Learning on Edge. , 2022, , 115-135.		0
1315	Atomic Dataflow based Graph-Level Workload Orchestration for Scalable DNN Accelerators. , 2022, , .		9
1316	THETA: A High-Efficiency Training Accelerator for DNNs With Triple-Side Sparsity Exploration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1034-1046.	3.1	5
1317	A Cross-Disciplinary Outlook of Directions and Challenges in Industrial Electronics. IEEE Open Journal of the Industrial Electronics Society, 2022, 3, 375-391.	6.8	0
1318	DTQAtten: Leveraging Dynamic Token-based Quantization for Efficient Attention Architecture. , 2022, , .		6
1319	ENCORE Compression: Exploiting Narrow-width Values for Quantized Deep Neural Networks. , 2022, , .		5
1320	TCX: A Programmable Tensor Processor. , 2022, , .		0
1321	Value-aware Parity Insertion ECC for Fault-tolerant Deep Neural Network. , 2022, , .		7
1322	Triple-Skipping Near-MRAM Computing Framework for AIoT Era. , 2022, , .		1
1323	MEDEA: A Multi-objective Evolutionary Approach to DNN Hardware Mapping. , 2022, , .		3

#	Article	IF	Citations
1324	RedMulE: A Compact FP16 Matrix-Multiplication Accelerator for Adaptive Deep Learning on RISC-V-Based Ultra-Low-Power SoCs. , 2022, , .		6
1325	DASC: A DRAM Data Mapping Methodology for Sparse Convolutional Neural Networks. , 2022, , .		0
1326	Algorithm-Hardware Co-Design for Efficient Brain-Inspired Hyperdimensional Learning on Edge. , 2022, , .		7
1327	An ASIP for Neural Network Inference on Embedded Devices with 99% PE Utilization and 100% Memory Hidden under Low Silicon Cost. Sensors, 2022, 22, 3841.	3.8	0
1328	Sigmoid Activation Implementation for Neural Networks Hardware Accelerators Based on Reconfigurable Computing Environments for Low-Power Intelligent Systems. Applied Sciences (Switzerland), 2022, 12, 5216.	2.5	2
1329	Biomechanical Analysis of Martial Arts Movements Based on Improved PSO Optimized Neural Network. Mobile Information Systems, 2022, 2022, 1-12.	0.6	1
1330	RED++ : Data-Free Pruning of Deep Neural Networks via Input Splitting and Output Merging. IEEE Transactions on Pattern Analysis and Machine Intelligence, 2023, 45, 3664-3676.	13.9	1
1331	FitNN: A Low-Resource FPGA-Based CNN Accelerator for Drones. IEEE Internet of Things Journal, 2022, 9, 21357-21369.	8.7	10
1332	Algorithm/Accelerator Co-Design and Co-Search for Edge AI. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3064-3070.	3.0	2
1333	RNA: A Flexible and Efficient Accelerator Based on Dynamically Reconfigurable Computing for Multiple Convolutional Neural Networks. Journal of Circuits, Systems and Computers, 2022, 31, .	1.5	1
1334	Physical Compact Model for Threeâ€Terminal SONOS Synaptic Circuit Element. Advanced Intelligent Systems, 2022, 4, .	6.1	2
1335	Recognition Accuracy Enhancement using Interface Control with Weight Variation-Lowering in Analog Computation-in-Memory. , 2022, , .		0
1336	High-Throughput and Power-Efficient Convolutional Neural Network Using One-Pass Processing Elements. Journal of Circuits, Systems and Computers, 2022, 31, .	1.5	5
1337	Anticipating and eliminating redundant computations in accelerated sparse training. , 2022, , .		2
1338	P3S: A High Accuracy Probabilistic Prediction Processing System for CNN Acceleration. , 2022, , .		0
1339	(Retracted) Image recognition technology of crop diseases based on neural network model fusion. Journal of Electronic Imaging, 2022, 32, .	0.9	1
1340	uBrain. , 2022, , .		4
1341	Reducing Power Consumption using Approximate Encoding for CNN Accelerators at the Edge. , 2022, , .		1

#	Article	IF	Citations
1342	DTATrans: Leveraging Dynamic Token-Based Quantization With Accuracy Compensation Mechanism for Efficient Transformer Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 509-520.	2.7	1
1343	A Programmable and Flexible Vision Processor. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3884-3888.	3.0	4
1344	A 184-Î¼W Error-Tolerant Real-Time Hand Gesture Recognition System With Hybrid Tiny Classifiers Utilizing Edge CNN. IEEE Journal of Solid-State Circuits, 2023, 58, 530-542.	5.4	4
1345	Dynamic Rate Neural Acceleration Using Multiprocessing Mode Support. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1461-1472.	3.1	0
1346	An FPGA-Based Energy-Efficient Reconfigurable Depthwise Separable Convolution Accelerator for Image Recognition. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 4003-4007.	3.0	7
1347	Trainer: An Energy-Efficient Edge-Device Training Processor Supporting Dynamic Weight Pruning. IEEE Journal of Solid-State Circuits, 2022, 57, 3164-3178.	5.4	5
1348	Approximations in Deep Learning. , 2022, , 467-512.		2
1349	Bayesian Photonic Accelerators for Energy Efficient and Noise Robust Neural Processing. IEEE Journal of Selected Topics in Quantum Electronics, 2022, 28, 1-10.	2.9	3
1350	DyNNamic: Dynamically Reshaping, High Data-Reuse Accelerator for Compact DNNs. IEEE Transactions on Computers, 2023, 72, 880-892.	3.4	0
1351	High-Efficiency Data Conversion Interface for Reconfigurable Function-in-Memory Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1193-1206.	3.1	3
1352	Special Session: Effective In-field Testing of Deep Neural Network Hardware Accelerators. , 2022, , .		0
1353	Reconfigurable Architecture for Real-time Decoding of Canonical Huffman Codes. , 2022, , .		0
1354	Miniaturization for wearable EEG systems: recording hardware and data processing. Biomedical Engineering Letters, 2022, 12, 239-250.	4.1	3
1355	Ultra-Low-Power Modulo Adder with Thermometer Coding for Uncertain RNS Applications. Journal of Uncertain Systems, 2022, 15, .	0.7	0
1356	Trainable Communication Systems Based on the Binary Neural Network. Frontiers in Communications and Networks, 0, 3, .	3.0	1
1357	Efficient hardware design of a deep U-net model for pixel-level ECG classification in healthcare device. Microelectronics Journal, 2022, 126, 105492.	2.0	9
1359	Sample-Wise Dynamic Precision Quantization for Neural Network Acceleration. IEICE Electronics Express, 2022, , .	0.8	0
1360	Data Rearrange Unit for Efficient Data Computation. International Journal of Networking and Computing, 2022, 12, 295-316.	0.4	0

#	Article	IF	Citations
1361	AIDA: Associative In-Memory Deep Learning Accelerator. IEEE Micro, 2022, 42, 67-75.	1.8	10
1363	Unleashing the Potential of Sparse DNNs Through Synergistic Hardware-Sparsity Co-Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 1147-1160.	2.7	2
1365	Memristor-based Deep Spiking Neural Network with a Computing-In-Memory Architecture. , 2022, , .		9
1366	Analysis of the Effect of Off-chip Memory Access on the Performance of an NPU System. , 2022, , .		1
1367	Bifrost: End-to-End Evaluation and optimization of Reconfigurable DNN Accelerators. , 2022, , .		2
1368	A Method Executing Optical Real-Valued Matrix Multiplication. , 2022, , .		0
1369	A Formalism of DNN Accelerator Flexibility. Proceedings of the ACM on Measurement and Analysis of Computing Systems, 2022, 6, 1-23.	1.8	0
1370	SaARSP: An Architecture for Systolic-Array Acceleration of Recurrent Spiking Neural Networks. ACM Journal on Emerging Technologies in Computing Systems, 2022, 18, 1-23.	2.3	1
1371	Computation and memory optimized spectral domain convolutional neural network for throughput and energy-efficient inference. Applied Intelligence, 0, , .	5.3	0
1372	A high-performance, hardware-based deep learning system for disease diagnosis. PeerJ Computer Science, 0, 8, e1034.	4.5	1
1373	Design Framework for ReRAM-Based DNN Accelerators with Accuracy and Hardware Evaluation. Electronics (Switzerland), 2022, 11, 2107.	3.1	1
1374	DCNN search and accelerator co-design: Improve the adaptability between NAS frameworks and embedded platforms. The Integration VLSI Journal, 2022, , .	2.1	2
1375	Breaking Barriers: Maximizing Array Utilization for Compute in-Memory Fabrics. , 2020, , .		1
1378	Accelerating deep neural network filter pruning with mask-aware convolutional computations on modern CPUs. Neurocomputing, 2022, 505, 375-387.	5.9	4
1380	A 40.96-GOPS 196.8-mW Digital Logic Accelerator Used in DNN for Underwater Object Recognition. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 4860-4871.	5.4	1
1381	A Novel Low-Power Compression Scheme for Systolic Array-Based Deep Learning Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 1085-1098.	2.7	1
1382	Digital Versus Analog Artificial Intelligence Accelerators: Advances, trends, and emerging designs. IEEE Solid-State Circuits Magazine, 2022, 14, 65-79.	0.4	18
1383	Clustered Network Adaptation Methodology for the Resource Constrained Platform. , 2022, , .		0

#	Article	IF	Citations
1384	Terminator on SkyNet. , 2022, , .		1
1385	Dataflow Optimization through Exploring Single-Layer and Inter-Layer Data Reuse in Memory-Constrained Accelerators. Electronics (Switzerland), 2022, 11, 2356.	3.1	0
1386	A computing-in-memory macro based on three-dimensional resistive random-access memory. Nature Electronics, 2022, 5, 469-477.	26.0	51
1387	Design and Acceleration of Field Programmable Gate Array-Based Deep Learning for Empty-Dish Recycling Robots. Applied Sciences (Switzerland), 2022, 12, 7337.	2.5	4
1388	Generating Efficient FPGA-based CNN Accelerators from High-Level Descriptions. Journal of Signal Processing Systems, 0, , .	2.1	0
1389	Performance Estimation of Photonic Neural Network Accelerator with Magneto-optical Switch Array. , 2022, , .		0
1390	Meta-optic accelerators for object classifiers. Science Advances, 2022, 8, .	10.3	17
1391	A hardware-efficient computing engine for FPGA-based deep convolutional neural network accelerator. Microelectronics Journal, 2022, 128, 105547.	2.0	6
1392	Remote sensing data processing and analysis for the identification of geological entities. Acta Geophysica, 2023, 71, 1565-1577.	2.0	3
1393	Time-Constrained Adversarial Defense in IoT Edge Devices through Kernel Tensor Decomposition and Multi-DNN Scheduling. Sensors, 2022, 22, 5896.	3.8	0
1394	Godiva: green on-chip interconnection for DNNs. Journal of Supercomputing, 0, , .	3.6	0
1395	A compute-in-memory chip based on resistive random-access memory. Nature, 2022, 608, 504-512.	27.8	210
1396	Unified energy-efficient reconfigurable MAC for dynamic Convolutional Neural Network based on Winograd algorithm. Microprocessors and Microsystems, 2022, 93, 104624.	2.8	1
1397	EALI: Energy-aware layer-level scheduling for convolutional neural network inference services on GPUs. Neurocomputing, 2022, 507, 265-281.	5.9	2
1398	Cerebron: A Reconfigurable Architecture for Spatiotemporal Sparse Spiking Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1425-1437.	3.1	6
1399	Asrpu: A Programmable Accelerator for Low-Power Automatic Speech Recognition. SSRN Electronic Journal, 0, , .	0.4	0
1400	A Survey of Intelligent Chip Design Research Based on Spiking Neural Networks. IEEE Access, 2022, 10, 89663-89686.	4.2	3
1401	Efficient Discrete Temporal Coding Spike-Driven In-Memory Computing Macro for Deep Neural Network Based on Nonvolatile Memory. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 4487-4498.	5.4	2

#	Article	IF	Citations
1402	Electrically Small, Cooling-Enhanced, Ungrounded Shielding Gasket for Compact and Wideband Integrated Circuits. IEEE Transactions on Electromagnetic Compatibility, 2022, 64, 1632-1640.	2.2	1
1403	Optimization of Scatter Network Architectures and Bank Allocations for Sparse CNN Accelerators. IEEE Access, 2022, 10, 85864-85879.	4.2	0
1404	TRIM: A Design Space Exploration Model for Deep Neural Networks Inference and Training Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, , 1-1.	2.7	0
1405	SamurAI: A Versatile IoT Node With Event-Driven Wake-Up and Embedded ML Acceleration. IEEE Journal of Solid-State Circuits, 2023, 58, 1782-1797.	5.4	5
1406	A Proposal forÂFPGA-Accelerated Deep Learning Ensembles inÂMPSoC Platforms Applied toÂMalware Detection. Communications in Computer and Information Science, 2022, , 239-249.	0.5	0
1407	A 389 TOPS/W, Always ON Region Proposal Integrated Circuit Using In-Memory Computing in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2023, 58, 554-568.	5.4	3
1408	An FPGA-Based Transformer Accelerator Using Output Block Stationary Dataflow for Object Recognition Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 281-285.	3.0	4
1409	A 28 nm 81 Kb 59â€“95.3 TOPS/W 4T2R ReRAM Computing-in-Memory Accelerator With Voltage-to-Time-to-Digital Based Output. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 846-857.	3.6	2
1410	ENOS: Energy-Aware Network Operator Search in Deep Neural Networks. IEEE Access, 2022, 10, 81447-81457.	4.2	8
1411	A 4.4â€“75-TOPS/W 14-nm Programmable, Performance- and Precision-Tunable All-Digital Stochastic Computing Neural Network Inference Accelerator. IEEE Solid-State Circuits Letters, 2022, 5, 206-209.	2.0	4
1412	Scalable 2T2R Logic Computation Structure: Design From Digital Logic Circuits to 3-D Stacked Memory Arrays. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2022, 8, 84-92.	1.5	1
1413	Achieving the Performance of All-Bank In-DRAM PIM With Standard Memory Interface: Memory-Computation Decoupling. IEEE Access, 2022, 10, 93256-93272.	4.2	3
1414	Edge AI: Leveraging the Full Potential of Deep Learning. Studies in Computational Intelligence, 2022, , 27-46.	0.9	5
1415	Exploiting Beam Search Confidence for Energy-Efficient Speech Recognition. SSRN Electronic Journal, 0, , .	0.4	0
1416	Collaborative Deep Neural Network Inference via Mobile Edge Computing. Wireless Networks, 2022, , 263-290.	0.5	0
1417	Design of Efficient AI Accelerator Building Blocks in Quantum-Dot Cellular Automata (QCA). IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 703-712.	3.6	2
1418	APTPU: Approximate Computing Based Tensor Processing Unit. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 5135-5146.	5.4	5
1419	Comparison of Different Deployment Approaches of FPGA-Based Hardware Accelerator for 3D Object Detection Models. Lecture Notes in Computer Science, 2022, , 285-296.	1.3	2

#	Article	IF	Citations
1420	GRIP: A Graph Neural Network Accelerator Architecture. IEEE Transactions on Computers, 2023, 72, 914-925.	3.4	12
1421	Neural Architecture Search for Transformers: A Survey. IEEE Access, 2022, 10, 108374-108412.	4.2	10
1422	Efficient Approximate DNN Accelerators for Edge Devices: An Experimental Study. , 2022, , 481-508.		0
1423	On-the-Fly Lowering Engine: Offloading Data Layout Conversion for Convolutional Neural Networks. IEEE Access, 2022, 10, 79730-79746.	4.2	1
1424	HD-CIM: Hybrid-Device Computing-In-Memory Structure Based on MRAM and SRAM to Reduce Weight Loading Energy of Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 4465-4474.	5.4	7
1425	SASCHAâ€"Sparsity-Aware Stochastic Computing Hardware Architecture for Neural Network Acceleration. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4169-4180.	2.7	2
1426	A Fast, Accurate, and Comprehensive PPA Estimation of Convolutional Hardware Accelerators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 5171-5184.	5.4	3
1427	NVP: A Flexible and Efficient Processor Architecture for Accelerating Diverse Computer Vision Tasks including DNN. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 271-275.	3.0	0
1428	Multiobjective End-to-End Design Space Exploration of Parameterized DNN Accelerators. IEEE Internet of Things Journal, 2023, 10, 1800-1812.	8.7	0
1429	Application of an Improved Clustering Algorithm of Neural Networks in Performance Appraisal Systems. Journal of Cases on Information Technology, 2022, 24, 1-20.	0.7	1
1430	MAPPARAT: A Resource Constrained FPGA-Based Accelerator for Sparse-Dense Matrix Multiplication. , 2022, , .		0
1431	Atrial Fibrillation Detection Using Weight-Pruned, Log-Quantised Convolutional Neural Networks. , 2022, , .		1
1432	Bin-Specific Quantization in Spectral-Domain Convolutional Neural Network Accelerators. , 2022, , .		0
1433	Extensible and Modularized Processing Unit Design and Implementation for AI Accelerator. , 2022, , .		0
1434	Row-wise Accelerator for Vision Transformer. , 2022, , .		4
1435	Hetero Layer Fusion Based Architecture Design and Implementation for of Deep Learning Accelerator. , 2022, , .		1
1436	Energy-Efficient Deep Neural Network Optimization via Pooling-Based Input Masking. , 2022, , .		0
1437	StarLight: a photonic neural network accelerator featuring a hybrid mode-wavelength division multiplexing and photonic nonvolatile memory. Optics Express, 2022, 30, 37051.	3.4	9

#	Article	IF	Citations
1438	VLSI Architecture for Image Scaling in Multimedia Applications. Advances in Intelligent Systems and Computing, 2023, , 423-433.	0.6	0
1439	Arbitrary surface data patching method based on geometric convolutional neural network. Neural Computing and Applications, 0, , .	5.6	1
1440	Reconfigurable Compute-In-Memory on Field-Programmable Ferroelectric Diodes. Nano Letters, 2022, 22, 7690-7698.	9.1	17
1441	HW-Flow-Fusion: Inter-Layer Scheduling for Convolutional Neural Network Accelerators with Dataflow Architectures. Electronics (Switzerland), 2022, 11, 2933.	3.1	2
1442	Compiling CNNs with Cain: focal-plane processing for robot navigation. Autonomous Robots, 0, , .	4.8	2
1443	Automatic Modulation Classification with Neural Networks via Knowledge Distillation. Electronics (Switzerland), 2022, 11, 3018.	3.1	0
1444	Development of a generalized model for parallel-streaming neural element and structures for scalar product calculation devices. Journal of Supercomputing, 2023, 79, 4820-4846.	3.6	2
1445	Detecting Functional Safety Violations in Online AI Accelerators. , 2022, , .		1
1446	QUIDAM: A Framework for <u>Qu</u> ant <u>i</u> zation-aware <u>D</u> NN <u>A</u> ccelerator and <u>M</u> odel Co-Exploration. Transactions on Embedded Computing Systems, 2023, 22, 1-21.	2.9	0
1448	A Non-Idealities Aware Softwareâ€“Hardware Co-Design Framework for Edge-AI Deep Neural Network Implemented on Memristive Crossbar. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 934-943.	3.6	5
1449	Area Efficient Compression for Floating-Point Feature Maps in Convolutional Neural Network Accelerators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 746-750.	3.0	1
1450	RDO-Q: Extremely Fine-Grained Channel-Wise Quantization viaÂRate-Distortion Optimization. Lecture Notes in Computer Science, 2022, , 157-172.	1.3	1
1451	SATA: Sparsity-Aware Training Accelerator for Spiking Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 1926-1938.	2.7	5
1452	Non-uniform Step Size Quantization for Accurate Post-training Quantization. Lecture Notes in Computer Science, 2022, , 658-673.	1.3	1
1453	PalQuant: Accelerating High-Precision Networks onÂLow-Precision Accelerators. Lecture Notes in Computer Science, 2022, , 312-327.	1.3	0
1454	Weight Fixing Networks. Lecture Notes in Computer Science, 2022, , 415-431.	1.3	1
1455	An Uninterrupted Processing Technique-Based High-Throughput and Energy-Efficient Hardware Accelerator for Convolutional Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1891-1901.	3.1	2
1456	3D Point Cloud Semantic Segmentation System. , 2022, , .		1

#	Article	IF	Citations
1457	A New Hardware-Efficient VLSI-Architecture of GoogLeNet CNN-Model Based Hardware Accelerator for Edge Computing Applications. , 2022, , .		1
1458	Low Complexity Reconfigurable-Scalable Architecture Design Methodology for Deep Neural Network Inference Accelerator. , 2022, , .		0
1459	Cache-locality Based Adaptive Warp Scheduling for Neural Network Acceleration on GPGPUs. , 2022, , .		0
1460	Work-in-Progress: Ultra-fast yet Accurate Performance Prediction for Deep Neural Network Accelerators. , 2022, , .		0
1461	Neural network learning using non-ideal resistive memory devices. Frontiers in Nanotechnology, 0, 4, .	4.8	4
1462	TCX: A RISC Style Tensor Computing Extension and a Programmable Tensor Processor. Transactions on Embedded Computing Systems, 2023, 22, 1-27.	2.9	1
1463	Work-in-Progress: NoRF: A Case Against Register File Operands in Tightly-Coupled Accelerators. , 2022, , .		0
1464	A Reconfigurable Deep Neural Network on Chip Design with Flexible Convolutional Operations. , 2022, , .		0
1465	Segmentation Algorithm of Magnetic Resonance Imaging Glioma under Fully Convolutional Densely Connected Convolutional Networks. Stem Cells International, 2022, 2022, 1-9.	2.5	1
1466	Delocalized photonic deep learning on the internetâ€™s edge. Science, 2022, 378, 270-276.	12.6	46
1467	Efficiency analysis of artificial vs. Spiking Neural Networks on FPGAs. Journal of Systems Architecture, 2022, 133, 102765.	4.3	4
1468	Sparseloop: An Analytical Approach To Sparse Tensor Accelerator Modeling. , 2022, , .		6
1469	A fine-grained mixed precision DNN accelerator using a two-stage bigâ€“little core RISC-V MCU. The Integration VLSI Journal, 2023, 88, 241-248.	2.1	0
1470	ANNA: Accelerating Neural Network Accelerator through software-hardware co-design for vertical applications in edge systems. Future Generation Computer Systems, 2023, 140, 91-103.	7.5	1
1471	PIMCA: A Programmable In-Memory Computing Accelerator for Energy-Efficient DNN Inference. IEEE Journal of Solid-State Circuits, 2023, 58, 1436-1449.	5.4	4
1472	Are SNNs Really More Energy-Efficient Than ANNs? an In-Depth Hardware-Aware Study. IEEE Transactions on Emerging Topics in Computational Intelligence, 2023, 7, 731-741.	4.9	6
1473	A 64 TOPS Energy-Efficient Tensor Accelerator in 14nm with Reconfigurable Fetch Network and Processing Fusion for Maximal Data Reuse. IEEE Open Journal of the Solid-State Circuits Society, 2022, , 1-1.	2.7	0
1474	Energy-Efficient DNN Training Processors on Micro-AI Systems. IEEE Open Journal of the Solid-State Circuits Society, 2022, 2, 259-275.	2.7	4

#	Article	IF	Citations
1475	A Systolic Neural CPU Processor Combining Deep Learning and General-Purpose Computing With Enhanced Data Locality and End-to-End Performance. IEEE Journal of Solid-State Circuits, 2023, 58, 216-226.	5.4	2
1476	A Lightweight Spiking GAN Model for Memristor-centric Silicon Circuit with On-chip Reinforcement Adversarial Learning. , 2022, , .		1
1477	Deep Neural Network Interlayer Feature Map Compression Based on Least-Squares Fitting. , 2022, , .		1
1478	Dynamically Swappable Digit-Serial Multi-Precision Deep Neural Network Accelerator with Early Termination. , 2022, , .		0
1479	A 65nm Compute-In-Memory 7T SRAM Macro Supporting 4-bit Multiply and Accumulate Operation by Employing Charge Sharing. , 2022, , .		3
1480	High Level Synthesis Acceleration of Change Detection in Multi-Temporal High Resolution Sentinel-2 Satellite Images. , 2022, , .		0
1481	ZaLoBI: Zero avoiding Load Balanced Inference accelerator. , 2022, , .		1
1482	Industry-track: Towards Agile Design of Neural Processing Unit. , 2022, , .		1
1483	GAPCNN with HyPar: Global Average Pooling convolutional neural network with novel NNLU activation function and HYBRID parallelism. Frontiers in Computational Neuroscience, 0, 16, .	2.1	2
1484	Technical Difficulties and Development Trend. , 2023, , 135-166.		0
1485	Floating Gate Transistorâ€Based Accurate Digital Inâ€Memory Computing for Deep Neural Networks. Advanced Intelligent Systems, 0, , 2200127.	6.1	1
1486	Recent Developments in Low-Power AI Accelerators: A Survey. Algorithms, 2022, 15, 419.	2.1	4
1487	Resistive-RAM-Based In-Memory Computing for Neural Network: A Review. Electronics (Switzerland), 2022, 11, 3667.	3.1	8
1488	Optical neural ordinary differential equations. Optics Letters, 2023, 48, 628.	3.3	2
1489	GANDSE: Generative Adversarial Network-based Design Space Exploration for Neural Network Accelerator Design. ACM Transactions on Design Automation of Electronic Systems, 2023, 28, 1-20.	2.6	1
1490	A Systematic Survey of General Sparse Matrix-matrix Multiplication. ACM Computing Surveys, 2023, 55, 1-36.	23.0	9
1491	Evaluation Platform of Time-Domain Computing-in-Memory Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 1174-1178.	3.0	3
1492	A Transistor Operations Model for Deep Learning Energy Consumption Scaling Law. IEEE Transactions on Artificial Intelligence, 2024, 5, 192-204.	4.7	0

#	Article	IF	Citations
1493	An Eight-Core RISC-V Processor With Compute Near Last Level Cache in Intel 4 CMOS. IEEE Journal of Solid-State Circuits, 2023, 58, 1117-1128.	5.4	5
1494	Efficient Hardware Architectures for Accelerating Deep Neural Networks: Survey. IEEE Access, 2022, 10, 131788-131828.	4.2	14
1495	ADC-Free ReRAM-Based In-Situ Accelerator for Energy-Efficient Binary Neural Networks. IEEE Transactions on Computers, 2024, 73, 353-365.	3.4	3
1496	Bottleneck-Stationary Compact Model Accelerator With Reduced Requirement on Memory Bandwidth for Edge Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2023, 70, 772-782.	5.4	1
1497	A Heterogeneous and Programmable Compute-In-Memory Accelerator Architecture for Analog-AI Using Dense 2-D Mesh. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, 31, 114-127.	3.1	14
1498	PTTS: Power-aware tensor cores using two-sided sparsity. Journal of Parallel and Distributed Computing, 2023, 173, 70-82.	4.1	2
1499	A Brain-Inspired ADC-Free SRAM-Based In-Memory Computing Macro With High-Precision MAC for AI Application. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 1276-1280.	3.0	3
1500	Efficient Acceleration of Deep Learning Inference on Resource-Constrained Edge Devices: A Review. Proceedings of the IEEE, 2023, 111, 42-91.	21.3	18
1501	Fault-Free: A Framework for Analysis and Mitigation of Stuck-At-Fault on Realistic ReRAM-Based DNN Accelerators. IEEE Transactions on Computers, 2022, , 1-14.	3.4	2
1502	Reconfigurability, Why It Matters in AI Tasks Processing: A Survey of Reconfigurable AI Chips. IEEE Transactions on Circuits and Systems I: Regular Papers, 2023, 70, 1228-1241.	5.4	1
1503	A Novel Predictor with Optimized Sampling Method for Hardware-aware NAS. , 2022, , .		0
1504	Cost-Aware TVM (CAT) Tensorization for Modern Deep Learning Accelerators. , 2022, , .		0
1505	VEA: An FPGA-Based Voxel Encoding Accelerator for 3D Object Detection with LiDAR. , 2022, , .		0
1506	Design Methodology and Trends of SRAM-Based Compute-in-Memory Circuits. , 2022, , .		1
1507	A Multibit MAC Scheme using Switched Capacitor based 3C Multiplier for Analog Compute In-Memory Architecture. , 2022, , .		2
1508	Deep Learning Toolkit-Accelerated Analytical Co-Optimization of CNN Hardware and Dataflow. , 2022, , .		1
1509	DNNCloak: Secure DNN Models Against Memory Side-channel Based Reverse Engineering Attacks. , 2022, , .		1
1510	Energy-efficient and Accurate Object Detection Design on an FPGA Platform. , 2022, , .		0

#	Article	IF	Citations
1511	NASA. , 2022, , .		1
1512	Area Reduction in Field Programmable Gate Array with Convolutional Neural Network. , 2022, , .		0
1513	Comparing the performance of multi-layer perceptron training on electrical and optical network-on-chips. Journal of Supercomputing, 2023, 79, 10725-10746.	3.6	3
1514	Scale-out Systolic Arrays. Transactions on Architecture and Code Optimization, 2023, 20, 1-25.	2.0	4
1515	gSuite: A Flexible and Framework Independent Benchmark Suite for Graph Neural Network Inference on GPUs. , 2022, , .		0
1516	ICARUS. ACM Transactions on Graphics, 2022, 41, 1-14.	7.2	13
1517	A Compact Butterfly-Style Silicon Photonicâ€“Electronic Neural Chip for Hardware-Efficient Deep Learning. ACS Photonics, 2022, 9, 3906-3916.	6.6	15
1518	Feasibility Analysis and Implementation of Adaptive Dynamic Reconfiguration of CNN Accelerators. Electronics (Switzerland), 2022, 11, 3805.	3.1	1
1519	Unified Buffer: Compiling Image Processing and Machine Learning Applications to Push-Memory Accelerators. Transactions on Architecture and Code Optimization, 2023, 20, 1-26.	2.0	2
1520	LUNG CANCER DETECTION BY HYBRID LEARNING METHOD APPLYING SMOTE TECHNIQUE. Gazi Ãœniversitesi Fen Bilimleri Dergisi, 0, , .	0.6	0
1521	An Energy-Efficient Convolutional Neural Network Processor Architecture Based on a Systolic Array. Applied Sciences (Switzerland), 2022, 12, 12633.	2.5	0
1522	Flexible Convolver for Convolutional Neural Networks Deployment onto Hardware-Oriented Applications. Applied Sciences (Switzerland), 2023, 13, 93.	2.5	0
1523	Energy Efficient Design of Coarse-Grained Reconfigurable Architectures: Insights, Trends and Challenges. , 2022, , .		0
1524	FPSNET: An Architecture for Neural-Network-Based Feature Point Extraction for SLAM. Electronics (Switzerland), 2022, 11, 4168.	3.1	1
1525	CNNFlow: Memory-driven Data Flow Optimization for Convolutional Neural Networks. ACM Transactions on Design Automation of Electronic Systems, 2023, 28, 1-36.	2.6	0
1526	Recognition method for stone carved calligraphy characters based on a convolutional neural network. Neural Computing and Applications, 0, , .	5.6	0
1527	TelaMalloc: Efficient On-Chip Memory Allocation for Production Machine Learning Accelerators. , 2022, , .		3
1528	PulseDL-II: A System-on-Chip Neural Network Accelerator for Timing and Energy Extraction of Nuclear Detector Signals. IEEE Transactions on Nuclear Science, 2023, 70, 971-978.	2.0	2

#	Article	IF	Citations
1529	A CNN Inference Accelerator on FPGA With Compression and Layer-Chaining Techniques for Style Transfer Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2023, 70, 1591-1604.	5.4	3
1530	An Area-Efficient Accelerator for Non-Maximum Suppression. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 2251-2255.	3.0	1
1531	Comparative Analysis of Energy Consumption in Text Processing Models. Communications in Computer and Information Science, 2022, , 107-116.	0.5	0
1532	An Energy-Efficient Accelerator for Medical Image Reconstruction From Implicit Neural Representation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2023, 70, 1625-1638.	5.4	1
1533	An Energy-and-Area-Efficient CNN Accelerator for Universal Powers-of-Two Quantization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2023, 70, 1242-1255.	5.4	4
1534	Development of DNN Accelerator and Its Application in Avionics System. Lecture Notes in Electrical Engineering, 2023, , 170-177.	0.4	0
1535	SparG: A Sparse GEMM Accelerator for Deep Learning Applications. Lecture Notes in Computer Science, 2023, , 529-547.	1.3	1
1536	Intelligent Computing: The Latest Advances, Challenges, and Future. , 2023, 2, .		26
1537	Freely switching between ferroelectric and resistive switching in Hf0.5Zr0.5O2 films and its application on high accuracy on-chip deep neural networks. Science China Information Sciences, 2023, 66, .	4.3	2
1538	A 1.6-mW Sparse Deep Learning Accelerator for Speech Separation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, 31, 310-319.	3.1	0
1539	Photonic machine learning with on-chip diffractive optics. Nature Communications, 2023, 14, .	12.8	41
1540	Optical Neural Network With Complementary Decomposition to Overcome the Phase Insensitive Constrains. IEEE Journal of Selected Topics in Quantum Electronics, 2023, 29, 1-8.	2.9	2
1541	A Charge Domain SRAM Compute-in-Memory Macro With C-2C Ladder-Based 8-Bit MAC Unit in 22-nm FinFET Process for Edge Inference. IEEE Journal of Solid-State Circuits, 2023, 58, 1037-1050.	5.4	10
1542	Ultralow-Power Implementation of Neural Networks Using Inverter-Based Memristive Crossbars. , 2023, , 327-385.		0
1543	Ferroelectric Content-Addressable Memory Cells with IGZO Channel: Impact of Retention Degradation on the Multibit Operation. ACS Applied Electronic Materials, 2023, 5, 812-820.	4.3	4
1544	STRAIT: Self-Test and Self-Recovery for AI Accelerator. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 3092-3104.	2.7	1
1545	TCADer: A Tightly Coupled Accelerator Design framework for heterogeneous system with hardware/software co-design. Journal of Systems Architecture, 2023, 136, 102822.	4.3	2
1546	Inference Time Reduction of Deep Neural Networks on Embedded Devices: A Case Study. , 2022, , .		2

#	Article	IF	Citations
1547	A Novel Image Processing System to Recognize and Classify Images using Integrated Advanced CNN and FPGA for IoT based Applications. , 2022, , .		0
1548	Magnitude and Similarity Based Variable Rate Filter Pruning for Efficient Convolution Neural Networks. Applied Sciences (Switzerland), 2023, 13, 316.	2.5	2
1549	An Adaptive Hardware Accelerator For Convolution Layers With Diverse Sizes. , 2022, , .		0
1550	Digital Computation-in-Memory Design with Adaptive Floating Point for Deep Neural Networks. , 2022, , .		0
1551	Energy Efficient Hardware Implementation of 2-D Convolution for Convolutional Neural Network. , 2022, , .		0
1553	NeuroCARE: A generic neuromorphic edge computing framework for healthcare applications. Frontiers in Neuroscience, 0, 17, .	2.8	5
1554	A Reconfigurable Spatial Architecture for Energy-Efficient Inception Neural Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2023, 13, 7-20.	3.6	1
1555	Design of Synaptic Driving Circuit for TFT eFlash-Based Processing-In-Memory Hardware Using Hybrid Bonding. Electronics (Switzerland), 2023, 12, 678.	3.1	0
1556	An In-Memory-Computing Charge-Domain Ternary CNN Classifier. IEEE Journal of Solid-State Circuits, 2023, 58, 1450-1461.	5.4	2
1557	Testability and Dependability of AI Hardware: Survey, Trends, Challenges, and Perspectives. IEEE Design and Test, 2023, 40, 8-58.	1.2	8
1558	A Bit-Serial, Compute-in-SRAM Design Featuring Hybrid-Integrating ADCs and Input Dependent Binary Scaled Precharge Eliminating DACs for Energy-Efficient DNN Inference. IEEE Journal of Solid-State Circuits, 2023, 58, 2109-2124.	5.4	1
1559	V-LSTM: An Efficient LSTM Accelerator Using Fixed Nonzero-Ratio Viterbi-Based Pruning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 3327-3337.	2.7	1
1560	TinyVers: A Tiny Versatile System-on-Chip With State-Retentive eMRAM for ML Inference at the Extreme Edge. IEEE Journal of Solid-State Circuits, 2023, 58, 2360-2371.	5.4	8
1561	Application Mapping Onto Manycore Processor Architectures Using Active Search Framework. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, 31, 789-801.	3.1	2
1562	Bit-Line Computing for CNN Accelerators Co-Design in Edge AI Inference. IEEE Transactions on Emerging Topics in Computing, 2023, 11, 358-372.	4.6	2
1563	Efficient Accelerator/Network Co-Search With Circular Greedy Reinforcement Learning. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 2615-2619.	3.0	3
1564	High-Frequency Systolic Array-Based Transformer Accelerator on Field Programmable Gate Arrays. Electronics (Switzerland), 2023, 12, 822.	3.1	1
1565	Application-Specific and Reconfigurable AI Accelerator. , 2023, , 183-223.		0

#	Article	IF	Citations
1566	Memory-Centric Fusion-based CNN Accelerator with 3D-NoC and 3D-DRAM. , 2022, , .		0
1567	Implementation of convolution layer in FPGA for disease classification in Tomato leaves. , 2022, , .		0
1568	A Binarized Systolic Array-Based Neuromorphic Architecture with High Efficiency. , 2022, , .		0
1569	Distributed Intelligence in Wireless Networks. IEEE Open Journal of the Communications Society, 2023, , 1-1.	6.9	3
1570	Integrated Optimization in Training Process for Binary Neural Network. , 2023, , .		0
1571	IXIAM: ISA EXtension for Integrated Accelerator Management. IEEE Access, 2023, 11, 33768-33791.	4.2	1
1572	A unifying review of edge intelligent computing technique applications in the field of energy networks. Journal of Industrial and Management Optimization, 2023, 19, 7966-7992.	1.3	2
1573	A Survey on Deep-Learning-Based Real-Time SAR Ship Detection. IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing, 2023, 16, 3218-3247.	4.9	9
1574	Sparse-Aware Deep Learning Accelerator. , 0, 39, 305-310.		0
1575	Evaluation of SEU impact on convolutional neural networks based on BRAM and CRAM in FPGAs. Microelectronics Reliability, 2023, 144, 114974.	1.7	0
1576	A Unified Engine for Accelerating GNN Weighting/Aggregation Operations, With Efficient Load Balancing and Graph-Specific Caching. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 4844-4857.	2.7	1
1577	The Impact of Cascaded Optimizations in CNN Models and End-Device Deployment. , 2022, , .		2
1578	Dataflow and Hardware Design for The Sharing of Feature Maps. , 2022, , .		0
1579	The Quantitative Comparisons of Analog and Digital SRAM Compute-In-Memories for Deep Neural Network Applications. , 2022, , .		0
1580	Performance-oriented FPGA-based convolution neural network designs. Multimedia Tools and Applications, 2023, 82, 21019-21030.	3.9	1
1582	Liquid-Based Memory Devices for Next-Generation Computing. ACS Applied Electronic Materials, 2023, 5, 664-673.	4.3	6
1583	NAND-SPIN-based processing-in-MRAM architecture for convolutional neural network acceleration. Science China Information Sciences, 2023, 66, .	4.3	3
1584	Sense: Model-Hardware Codesign for Accelerating Sparse CNNs on Systolic Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, 31, 470-483.	3.1	2

#	Article	IF	Citations
1585	Deep reinforcement learning-based pairwise DNA sequence alignment method compatible with embedded edge devices. Scientific Reports, 2023, 13, .	3.3	6
1586	Hybrid Signed Convolution Module With Unsigned Divide-and-Conquer Multiplier for Energy-Efficient STT-MRAM-Based AI Accelerator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, 31, 1078-1082.	3.1	3
1587	Flexer: Out-of-Order Scheduling for Multi-NPUs. , 2023, , .		2
1588	A New Constant Coefficient Multiplier for Deep Neural Network Accelerators. , 2022, , .		0
1589	Trouble-Shooting at GAN Point: Improving Functional Safety in Deep Learning Accelerators. IEEE Transactions on Computers, 2023, 72, 2194-2208.	3.4	2
1590	An On-Chip Fully Connected Neural Network Training Hardware Accelerator Based on Brain Float Point and Sparsity Awareness. IEEE Open Journal of Circuits and Systems, 2023, 4, 85-98.	1.9	5
1591	TRAM: An Open-Source Template-based Reconfigurable Architecture Modeling Framework. , 2022, , .		9
1592	A Generalized Residue Number System Design Approach for Ultralow-Power Arithmetic Circuits Based on Deterministic Bit-Streams. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 3787-3800.	2.7	3
1593	The Design of Efficient Data Flow and Low-Complexity Architecture for a Highly Configurable CNN Accelerator. Circuits, Systems, and Signal Processing, 0, , .	2.0	0
1594	Optimizing FPGA-Based Convolutional Neural Network Performance. Journal of Circuits, Systems and Computers, 2023, 32, .	1.5	0
1595	Quantitative Analysis of Various 2D CNN Structures based on Dataflow. , 2023, , .		0
1596	Radiation-Hardened Processing-In-Memory Crossbar Array With Hybrid Synapse Devices for Space Application. , 2023, , .		0
1597	ANS: Assimilating Near Similarity at High Accuracy for Significant Deduction of CNN Storage and Computation. IEEE Access, 2023, 11, 25415-25430.	4.2	0
1598	Multi-grained system integration for hybrid-paradigm brain-inspired computing. Science China Information Sciences, 2023, 66, .	4.3	2
1599	Resource-Efficient Convolutional Networks: A Survey on Model-, Arithmetic-, and Implementation-Level Techniques. ACM Computing Surveys, 2023, 55, 1-36.	23.0	2
1600	SAMBA: <u>S</u>parsity <u>A</u>ware In-<u>M</u>emory Computing <u>B</u>ased Machine Learning <u>A</u>ccelerator. IEEE Transactions on Computers, 2023, 72, 2615-2627.	3.4	3
1601	CNN Hardware Accelerator Architecture Design for Energy-Efficient AI. , 2023, , 319-357.		0
1602	Overviewing AI-Dedicated Hardware for On-Device AI in Smartphones. , 2023, , 127-150.		0

#	Article	IF	Citations
1603	AI Accelerators for Standalone Computer. , 2023, , 53-93.		0
1604	An FPGA-Based Computation-Efficient Convolutional Neural Network Accelerator. , 2022, , .		0
1605	DefT: Boosting Scalability of Deformable Convolution Operations on GPUs. , 2023, , .		0
1606	FlexDML: High Utilization Configurable Multimode Arithmetic Units Featuring Dual Mode Logic. IEEE Solid-State Circuits Letters, 2023, 6, 73-76.	2.0	2
1607	The Sparse Abstract Machine. , 2023, , .		6
1608	NASA+: Neural Architecture Search and Acceleration for Multiplication-Reduced Hybrid Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2023, 70, 2523-2536.	5.4	2
1609	The Hardware Impact of Quantization and Pruning for Weights in Spiking Neural Networks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 1789-1793.	3.0	2
1610	UArch: A Super-Resolution Processor With Heterogeneous Triple-Core Architecture for Workloads of U-Net Networks. IEEE Transactions on Biomedical Circuits and Systems, 2023, 17, 633-647.	4.0	2
1611	Agamotto: A Performance Optimization Framework for CNN Accelerator With Row Stationary Dataflow. IEEE Transactions on Circuits and Systems I: Regular Papers, 2023, 70, 2487-2496.	5.4	3
1612	An Efficient Accelerator Based on Lightweight Deformable 3D-CNN for Video Super-Resolution. IEEE Transactions on Circuits and Systems I: Regular Papers, 2023, 70, 2384-2397.	5.4	3
1613	Mix-GEMM: An efficient HW-SW Architecture for Mixed-Precision Quantized Deep Neural Networks Inference on Edge Devices. , 2023, , .		1
1614	VEGETA: Vertically-Integrated Extensions for Sparse/Dense GEMM Tile Acceleration on CPUs. , 2023, , .		1
1615	LightTrader: A Standalone High-Frequency Trading System with Deep Learning Inference Accelerators and Proactive Scheduler. , 2023, , .		2
1616	Charging Protocol for Partially Rechargeable Mobile Sensor Networks. Sensors, 2023, 23, 3438.	3.8	0
1617	TPCx-AI onÂNVIDIA Jetsons. Lecture Notes in Computer Science, 2023, , 49-66.	1.3	0
1618	An Energy-Constrained Optimization-Based Structured Pruning Method for Deep Neural Network Compression. , 2022, , .		0
1619	A dynamic computational memory address architecture for systolic array CNN accelerators. , 2022, , .		0
1620	ACBN: Approximate Calculated Batch Normalization for Efficient DNN On-Device Training Processor. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, , 1-11.	3.1	0

#	Article	IF	Citations
1621	A Ternary Neural Network Computing-In-Memory Processor with 16T1C Bitcell Architecture. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, , 1-1.	3.0	0
1622	Coarse-Grained High-speed Reconfigurable Array-based Approximate Accelerator for Deep Learning Applications. , 2023, , .		0
1623	SME: A Systolic Multiply-accumulate Engine for MLP-based Neural Network. , 2022, , .		0
1624	Ternary In-Memory MAC Accelerator With Dual-6T SRAM Cell for Deep Neural Networks. , 2022, , .		0
1625	Straightforward data transfer in a blockwise dataflow for an analog RRAM-based CIM system. Frontiers in Electronics, 0, 4, .	3.2	0
1626	Efficient Re-configurable Multiply and Accumulate Unit for Convolutional Neural Network. , 2022, , .		0
1627	A 218 GOPS neural network accelerator based on a novel cost-efficient surrogate gradient scheme for pattern classification. Microprocessors and Microsystems, 2023, , 104831.	2.8	1
1628	FPGA Based Area Reduction with Recurrent Neural Network and VHDL Modelling. , 2023, , .		0
1629	Two-Level Scheduling Algorithms for Deep Neural Network Inference in Vehicular Networks. IEEE Transactions on Intelligent Transportation Systems, 2023, 24, 9324-9343.	8.0	1
1630	A Fully Digital SRAM-Based Four-Layer In-Memory Computing Unit Achieving Multiplication Operations and Results Store. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, 31, 776-788.	3.1	2
1631	Design and Implementation of Convolutional Neural Network Accelerator Based on FPGA. , 2023, 3, 158-161.		1
1632	Dynamic Image Difficulty-Aware DNN Pruning. Micromachines, 2023, 14, 908.	2.9	0
1633	A Parallel Processing CNN Accelerator on Embedded Devices Based on Optimized MobileNet. IEEE Internet of Things Journal, 2023, 10, 18844-18852.	8.7	0
1634	ÐœÐ¾ÐŽÐµÐ»ÑŒ Ñ‚Ð° Ð¼ÐµÑ‚Ð¾Ð´ ÑŒÐ½Ñ‚ÐµÐ·Ð° Ð½ÐµÐ¹Ñ€Ð¾ÑƒÐ¿Ñ€Ð°Ð²Ð»ÑÐµÐ¼Ð¾Ð³Ð¾ ÐµÐ»ÐµÐ¼ÐµÐ½Ñ‚Ð°Ð¿Ð¿Ð°Ñ€Ð°Ñ‚Ð°		
1635	AccelTran: A Sparsity-Aware Accelerator for Dynamic Inference With Transformers. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 4038-4051.	2.7	2
1637	Memristive-based Mixed-signal CGRA for Accelerating Deep Neural Network Inference. ACM Transactions on Design Automation of Electronic Systems, 2023, 28, 1-25.	2.6	0
1638	A 4-Bit Mixed-Signal MAC Macro With One-Shot ADC Conversion. IEEE Journal of Solid-State Circuits, 2023, 58, 2648-2658.	5.4	0
1639	An Empirical Approach to Enhance Performance for Scalable CORDIC-Based Deep Neural Networks. ACM Transactions on Reconfigurable Technology and Systems, 2023, 16, 1-32.	2.5	1

#	Article	IF	Citations
1640	Trusted Deep Neural Executionâ€"A Survey. IEEE Access, 2023, 11, 45736-45748.	4.2	1
1641	Booth Encoded Bit-Serial Multiply-Accumulate Units with Improved Area and Energy Efficiencies. Electronics (Switzerland), 2023, 12, 2177.	3.1	0
1642	Compute-in-Memory Architecture. , 2023, , 1-40.		0
1643	DLA-E: a deep learning accelerator for endoscopic images classification. Journal of Big Data, 2023, 10, .	11.0	1
1644	HSB-GDM: a Hybrid Stochastic-Binary Circuit for Gradient Descent with Momentum in the Training of Neural Networks. , 2022, , .		0
1645	Precision and Performance-Aware Voltage Scaling in DNN Accelerators. , 2023, , .		0
1646	Heterogeneous Integration of In-Memory Analog Computing Architectures with Tensor Processing Units. , 2023, , .		0
1647	The CNN vs. SNN Event-camera Dichotomy and Perspectives For Event-Graph Neural Networks. , 2023, , .		0
1648	eF²lowSim: System-Level Simulator of eFlash-Based Compute-in-Memory Accelerators for Convolutional Neural Networks. , 2023, , .		0
1649	Prediction of Inference Energy on CNN Accelerators Supporting Approximate Circuits. , 2023, , .		0
1650	PRADA: Point Cloud Recognition Acceleration via Dynamic Approximation. , 2023, , .		0
1651	Emerging Memory Technologies for Data Storage and Brain-Inspired Computation: A Global View with Indian Research Insights with a Focus on Resistive Memories. Proceedings of the National Academy of Sciences India Section A - Physical Sciences, 0, , .	1.2	0
1652	FireFly: A High-Throughput Hardware Accelerator for Spiking Neural Networks With Efficient DSP and Memory Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, , 1-14.	3.1	1
1653	Joint Protection Scheme for Deep Neural Network Hardware Accelerators and Models. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 4518-4527.	2.7	0
1654	A 24.3 Î¼J/Image SNN Accelerator for DVS-Gesture With WS-LOS Dataflow and Sparse Methods. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 4226-4230.	3.0	1
1655	Reconfigurable Neuromorphic Computing: Materials, Devices, and Integration. Advanced Materials, 2023, 35, .	21.0	5
1656	NeuroSpector: Systematic Optimization of Dataflow Scheduling in DNN Accelerators. IEEE Transactions on Parallel and Distributed Systems, 2023, 34, 2279-2294.	5.6	0
1657	REX-SC: Range-Extended Stochastic Computing Accumulation for Neural Network Acceleration. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 4423-4435.	2.7	1

#	Article	IF	Citations
1658	TREAD-M3D: Temperature-Aware DNN Accelerators for Monolithic 3-D Mobile Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 4350-4363.	2.7	2
1659	An Energy-Efficient Bayesian Neural Network Accelerator With CiM and a Time-Interleaved Hadamard Digital GRNG Using 22-nm FinFET. IEEE Journal of Solid-State Circuits, 2023, , 1-13.	5.4	1
1660	Stack-YOLO: A Friendly-Hardware Real-Time Object Detection Algorithm. IEEE Access, 2023, 11, 62522-62534.	4.2	4
1661	Integrated Photonic Convolutional Neural Network Based on Silicon Metalines. IEEE Access, 2023, 11, 61728-61737.	4.2	1
1662	Programmable Olfactory Computing. , 2023, , .		0
1663	Energy Efficient Implementation of Processing Elements for CNN Hardware Accelerator. , 2023, , .		0
1664	Seizing the Bandwidth Scaling of On-Package Interconnect in a Post-Moore's Law World. , 2023, , .		1
1665	Modeling and optimizing PE utilization rate for systolic array based CNN accelerators. , 2023, , .		0
1666	A Runtime Switchable Multi-Phase Convolutional Neural Network for Resource-Constrained Systems. IEEE Access, 2023, 11, 62449-62461.	4.2	0
1667	Approximate Processing Element Design and Analysis for the Implementation of CNN Accelerators. Journal of Computer Science and Technology, 2023, 38, 309-327.	1.5	0
1668	Impact of Optimal Design Point on Performance Metrics of DNN accelerators in FPGA. , 2023, , .		0
1669	Stream: A Modeling Framework for Fine-grained Layer Fusion on Multi-core DNN Accelerators. , 2023, , .		0
1670	Advanced Topics in Deep Learning. , 2023, , 435-485.		0
1671	Design and Evaluation of Inexact Computation based Systolic Array for Convolution. , 2023, , .		0
1672	Boosting the Accuracy of SRAM-Based in-Memory Architectures Via Maximum Likelihood-Based Error Compensation Method. , 2023, , .		1
1673	Bedot: Bit Efficient Dot Product forÂDeep Generative Models. Lecture Notes in Computer Science, 2023, , 19-37.	1.3	0
1674	SpikeSim: An End-to-End Compute-in-Memory Hardware Evaluation Tool for Benchmarking Spiking Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 3815-3828.	2.7	6
1675	Saca-FI: A microarchitecture-level fault injection framework for reliability analysis of systolic array based CNN accelerator. Future Generation Computer Systems, 2023, 147, 251-264.	7.5	3

#	Article	IF	Citations
1676	Lightweight CNN-Based Low-Light-Image Enhancement System on FPGA Platform. Neural Processing Letters, 2023, 55, 8023-8039.	3.2	1
1677	Neuromorphic Accelerator for Deep Spiking Neural Networks with NVM Crossbar Arrays. , 2022, , .		0
1678	A High-Throughput Processor for GDN-Based Deep Learning Image Compression. Electronics (Switzerland), 2023, 12, 2289.	3.1	0
1679	Modeling and Library Support for Early-Stage Exploration of Sparse Tensor Accelerator Designs. IEEE Access, 2023, 11, 55361-55369.	4.2	0
1680	Reconfigurable spatial-parallel stochastic computing for accelerating sparse convolutional neural networks. Science China Information Sciences, 2023, 66, .	4.3	0
1681	HFGCN: High-speed and Fully-optimized GCN Accelerator. , 2023, , .		0
1682	Routability-aware Placement Guidance Generation for Mixed-size Designs. , 2023, , .		0
1683	Decomposable Architecture and Fault Mitigation Methodology for Deep Learning Accelerators. , 2023, , .		0
1684	Evaluation of architecture-aware optimization techniques for Convolutional Neural Networks. , 2023, , .		1
1685	DANNA: A Dimension-Aware Neural Network Accelerator for Unstructured Sparsity. , 2023, , .		0
1686	Implementation of Multiple Kernels for Edge Detection using Pipelined Architecture on FPGA. , 2023, , .		0
1687	Dedicated FPGA Implementation of the Gaussian TinyYOLOv3 Accelerator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 3882-3886.	3.0	1
1688	An Intelligent System With Reduced Readout Power and Lightweight CNN for Vision Applications. IEEE Transactions on Circuits and Systems for Video Technology, 2024, 34, 1310-1315.	8.3	0
1689	An Efficient CNN Inference Accelerator Based on Intra- and Inter-Channel Feature Map Compression. IEEE Transactions on Circuits and Systems I: Regular Papers, 2023, 70, 3625-3638.	5.4	1
1690	Rei: A Reconfigurable Interconnection Unit for Array-Based CNN Accelerators. IEEE Transactions on Emerging Topics in Computing, 2023, , 1-12.	4.6	0
1691	A digitally controlled switchedâ€ring oscillatorâ€based time domain multiplyâ€andâ€accumulate core for machine learning. International Journal of Circuit Theory and Applications, 0, , .	2.0	0
1692	Slimmer CNNs Through Feature Approximation and Kernel Size Reduction. IEEE Open Journal of Circuits and Systems, 2023, 4, 188-202.	1.9	0
1693	A Systolic Array with Activation Stationary Dataflow for Deep Fully-Connected Networks. , 2023, , .		0

#	Article	IF	Citations
1694	Convergent Waveform Relaxation Schemes for the Transient Analysis of Associative ReLU Arrays. , 2023, , .		0
1695	Simulation-driven Latency Estimations for Multi-core Machine Learning Accelerators. , 2023, , .		0
1696	A low-cost, high-throughput neuromorphic computer for online SNN learning. Cluster Computing, 0, , .	5.0	1
1697	Energy Efficient Software-hardware Co-design of Quantized Recurrent Convolutional Neural Network for Continuous Cardiac Monitoring. , 2023, , .		1
1698	Optimization Strategies for Digital Compute-in-Memory from Comparative Analysis with Systolic Array. , 2023, , .		3
1699	Survey on Activation Functions for Optical Neural Networks. ACM Computing Surveys, 2024, 56, 1-30.	23.0	1
1700	An Exploratory Study on Energy Consumption of Dataframe Processing Libraries. , 2023, , .		1
1701	An Electro-Photonic System for Accelerating Deep Neural Networks. ACM Journal on Emerging Technologies in Computing Systems, 2023, 19, 1-31.	2.3	6
1702	Irregular Workloads at Risk of Losing the Hardware Lottery. , 2023, , 1-21.		0
1703	Accelerating Distributed GNN Training by Codes. IEEE Transactions on Parallel and Distributed Systems, 2023, 34, 2598-2614.	5.6	0
1704	Integrated Imager and 3.22 Î¼s/Kernel-Latency All-Digital In-Imager Global-Parallel Binary Convolutional Neural Network Accelerator for Image Processing. IEEE Access, 2023, 11, 74364-74378.	4.2	1
1706	CSA Based Radix-4 Gemmini Systolic Array for Machine Learning Applications. , 2023, , .		1
1707	RRAM-PoolFormer: A Resistive Memristor-based PoolFormer Modeling and Training Framework for Edge-AI Applications. , 2023, , .		1
1708	Hardware Efficient Reconfigurable Logic-in-Memory Circuit Based Neural Network Computing. , 2023, , .		0
1709	GERALT: Real-time Detection of Evasion Attacks in Deep Learning Systems. , 2023, , .		0
1710	EACNN: Efficient CNN Accelerator Utilizing Linear Approximation and Computation Reuse. , 2023, , .		1
1711	High-frame rate homography and visual odometry by tracking binary features from the focal plane. Autonomous Robots, 0, , .	4.8	1
1712	Hardware deployment of deep learning model for classification of breast carcinoma from digital mammogram images. Medical and Biological Engineering and Computing, 2023, 61, 2843-2857.	2.8	0

#	Article	IF	Citations
1714	HNPU-V1: An Adaptive DNN Training Processor Utilizing Stochastic Dynamic Fixed-Point and Active Bit-Precision Searching. , 2023, , 121-161.		0
1715	DF-LNPU: A Pipelined Direct Feedback Alignment Based Deep Neural Network Learning Processor for Fast Online Learning. , 2023, , 95-119.		0
1716	Compare with the Traditional Heterogeneous Solution: Accelerate Neural Network Algorithm through Heterogeneous Integrated CPU+NPU Chip on Server. , 2023, , .		0
1717	An approach to the systematic characterization of multitask accelerated CNN inference in edge MPSoCs. Transactions on Embedded Computing Systems, 0, , .	2.9	0
1718	LETSCOPE: Lifecycle Extensions Through Software-Defined Predictive Control of Power Electronics. , 2023, , .		1
1719	Deep Learning ASIC Design. , 2023, , 201-224.		0
1720	SSM-CIM: An Efficient CIM Macro Featuring <u>S</u>ingle-<u>S</u>tep <u>M</u>ulti-bit MAC Computation for CNN Edge Inference. IEEE Transactions on Circuits and Systems I: Regular Papers, 2023, 70, 4357-4368.	5.4	0
1721	PDAVIS: Bio-inspired Polarization Event Camera. , 2023, , .		0
1722	Hardware-aware NAS by Genetic Optimisation with a Design Space Exploration Simulator. , 2023, , .		0
1723	A Fast Weight Control Strategy for Programmable Linear RAM Based on the Self-Calibrating Erase Operation. Electronics (Switzerland), 2023, 12, 3466.	3.1	0
1724	A wavelength-multiplexed photonic tensor processor based on Mach-Zehnder modulator. , 2023, , .		0
1725	Design of high performance and energy efficient convolution array for convolution neural network-based image inference engine. Engineering Applications of Artificial Intelligence, 2023, 126, 106953.	8.1	1
1726	Analysis of Optimum 3-Dimensional Array and Fast Data Movement for Efficient Memory Computation in Convolutional Neural Network Models. IFIP Advances in Information and Communication Technology, 2023, , 94-108.	0.7	0
1727	Integrated diffractive optical neural network with space-time interleaving. Chinese Optics Letters, 2023, 21, 091301.	2.9	2
1728	ELEMENT: Energy-Efficient Multi-NoP Architecture for IMC-Based 2.5-D Accelerator for DNN Training. IEEE Design and Test, 2023, 40, 51-63.	1.2	0
1729	Fast and Scalable Multicore YOLOv3-Tiny Accelerator Using Input Stationary Systolic Architecture. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, 31, 1774-1787.	3.1	0
1730	A NoC-Based Spatial DNN Inference Accelerator With Memory-Friendly Dataflow. IEEE Design and Test, 2023, 40, 39-50.	1.2	0
1731	An Efficient Convolutional Neural Network Accelerator. , 2023, , .		0

#	Article	IF	Citations
1732	A-DSCNN: Depthwise Separable Convolutional Neural Network Inference Chip Design Using an Approximate Multiplier. Chips, 2023, 2, 159-172.	1.4	1
1733	Advancements in On-Device Deep Neural Networks. Information (Switzerland), 2023, 14, 470.	2.9	1
1734	Neuromorphic applications in medicine. Journal of Neural Engineering, 2023, 20, 041004.	3.5	2
1735	Dependable DNN Accelerator for Safety-Critical Systems: A Review on the Aging Perspective. IEEE Access, 2023, 11, 89803-89834.	4.2	0
1736	A High Efficiency Hardware Accelerator for Convolution Neural Network. , 2023, , .		0
1737	System on Chip Testbed for Deep Neuromorphic Neural Networks. , 2023, , .		0
1738	Voltage Bias Scheme Optimization in FeFET Based Neural Network System. IEEE Electron Device Letters, 2023, 44, 1464-1467.	3.9	1
1739	DietCNN: Multiplication-free Inference for Quantized CNNs. , 2023, , .		0
1740	FAQ: Mitigating the Impact of Faults in the Weight Memory of DNN Accelerators through Fault-Aware Quantization. , 2023, , .		0
1741	Mitigating Memory Wall Effects in CNN Engines with On-the-Fly Weights Generation. ACM Transactions on Design Automation of Electronic Systems, 2023, 28, 1-31.	2.6	0
1742	Deep Reinforcement Learning Processor Design for Mobile Applications. , 2023, , 1-93.		0
1743	FPGA-based Deep Learning Inference Accelerators: Where Are We Standing?. ACM Transactions on Reconfigurable Technology and Systems, 2023, 16, 1-32.	2.5	2
1744	Resource-Efficient Neural Network Architectures for Classifying Nerve Cuff Recordings on Implantable Devices. IEEE Transactions on Biomedical Engineering, 2023, , 1-10.	4.2	3
1745	Online Quantization Adaptation forÂFault-Tolerant Neural Network Inference. Lecture Notes in Computer Science, 2023, , 243-256.	1.3	0
1746	Stuck-at Faults Tolerance and Recovery in MLP Neural Networks Using Imperfect Emerging CNFET Technology. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2023, 9, 168-175.	1.5	0
1747	HBP: Hierarchically Balanced Pruning and Accelerator Co-Design for Efficient DNN Inference. , 2023, , .		0
1748	When Monte-Carlo Dropout Meets Multi-Exit: Optimizing Bayesian Neural Networks on FPGA. , 2023, , .		0
1749	Hardwareâ€“Software Co-optimization Through Design Space Exploration. , 2024, , 59-69.		0

#	Article	IF	Citations
1750	High-Level Synthesis ofÂMemory Systems forÂDecoupled Data Orchestration. Lecture Notes in Computer Science, 2023, , 3-18.	1.3	0
1751	DIANA: DIgital and ANAlog Heterogeneous Multi-core System-on-Chip. , 2024, , 119-141.		0
1752	STRIVE: Enabling Choke Point Detection and Timing Error Resilience in a Low-Power Tensor Processing Unit. , 2023, , .		1
1753	PowerPruning: Selecting Weights and Activations for Power-Efficient Neural Network Acceleration. , 2023, , .		0
1754	TinyVers: A Tiny Versatile All-Digital Heterogeneous Multi-core System-on-Chip. , 2024, , 93-117.		0
1755	Design and Implementation of Convolutional Neural Network Image Recognition Acceleration System Based on FPGA. , 2023, , .		0
1756	Amber: A 16-nm System-on-Chip With a Coarse- Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra. IEEE Journal of Solid-State Circuits, 2024, 59, 947-959.	5.4	0
1757	PIM hardware accelerators for real-world problems. Advances in Computers, 2024, , 225-251.	1.6	0
1758	SG-Float: Achieving Memory Access and Computing Power Reduction Using Self-Gating Float in CNNs. Transactions on Embedded Computing Systems, 2023, 22, 1-22.	2.9	2
1759	Optimization of Microarchitecture and Dataflow for Sparse Tensor CNN Acceleration. IEEE Access, 2023, 11, 108818-108832.	4.2	2
1760	DIMCA: An Area-Efficient Digital In-Memory Computing Macro Featuring Approximate Arithmetic Hardware in 28 nm. IEEE Journal of Solid-State Circuits, 2024, 59, 960-971.	5.4	0
1761	OECS: a deep convolutional neural network accelerator based on a 3D hybrid optical-electrical NoC. Journal of Optical Communications and Networking, 2023, 15, 839.	4.8	0
1763	A Review of the Development of Artificial Intelligence Electronic Circuit Technology. Lecture Notes in Electrical Engineering, 2023, , 129-136.	0.4	0
1764	Efficient Deep Learning Using Non-volatile Memory Technology in GPU Architectures. , 2024, , 225-252.		2
1765	Breaking the energy-efficiency barriers for smart sensing applications with â€œSensing with Computingâ€• architectures. Science China Information Sciences, 2023, 66, .	4.3	0
1766	Massively Parallel Neural Processing Array (MPNA): A CNN Accelerator for Embedded Systems. , 2024, , 3-24.		0
1767	Efficient Hardware Acceleration of Emerging Neural Networks for Embedded Machine Learning: An Industry Perspective. , 2024, , 121-172.		1
1768	In-Memory Computing for AI Accelerators: Challenges and Solutions. , 2024, , 199-224.		0

#	Article	IF	Citations
1769	SimPyler: A Compiler-Based Simulation Framework for Machine Learning Accelerators. , 2023, , .		0
1770	ASLog: An Area-Efficient CNN Accelerator for Per-Channel Logarithmic Post-Training Quantization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2023, 70, 5380-5393.	5.4	0
1771	Exploiting Subword Permutations to Maximize CNN Compute Performance and Efficiency. , 2023, , .		0
1772	Custom ASICs for data center video processing: advancements in AI-ML integrated, high-performance VPUs for hyper-scaled platforms. , 2023, , .		0
1773	Nonlinear optical feature generator for machine learning. APL Photonics, 2023, 8, .	5.7	1
1774	Cross-Layer Optimizations for Efficient Deep Learning Inference at the Edge. , 2024, , 225-248.		0
1775	Algorithm-System Co-design for Efficient and Hardware-Aware Embedded Machine Learning. , 2024, , 349-370.		0
1776	Machine Learning Hardware Design for Efficiency, Flexibility, and Scalability [Feature]. IEEE Circuits and Systems Magazine, 2023, 23, 35-53.	2.3	0
1779	Accelerating Convolutional Neural Networks by Exploiting the Sparsity of Output Activation. IEEE Transactions on Parallel and Distributed Systems, 2023, , 1-14.	5.6	0
1780	Derin Ã–ÄŸrenme KullanÄ±larak Fundus GÃ¶rÃ¼ntÃ¼lerinden Katarakt ve Diyabetik Retinopati Tespiti. MÃ¼hendislik Bilimleri Ve AraÅŞtÄ±rmalarÄ± Dergisi, 0, , .	0.5	0
1781	AlPicoSoC: A Low-Power RISC-V Based System onÂChip forÂEdge Devices withÂaÂDeep Learning Accelerator. Lecture Notes on Data Engineering and Communications Technologies, 2023, , 403-413.	0.7	0
1782	A 5-mm², 4.7-Î¼W Convolutional Neural Network Layer Accelerator for Miniature Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, 31, 2142-2146.	3.1	0
1783	High-accuracy Low-latency Non-Maximum Suppression Processor for Traffic Object Detection. IEICE Electronics Express, 2023, , .	0.8	0
1784	Seizure-Cluster-Inception CNN (SciCNN): A Patient-Independent Epilepsy Tracking SoC with 0-Shot-Retraining. IEEE Transactions on Biomedical Circuits and Systems, 2023, , 1-12.	4.0	0
1785	POSS-CNN: An Automatically Generated Convolutional Neural Network with Precision and Operation Separable Structure Aiming at Target Recognition and Detection. Information (Switzerland), 2023, 14, 604.	2.9	0
1786	Accelerating AI performance with the incorporation of TVM and MediaTek NeuroPilot. Connection Science, 2023, 35, .	3.0	0
1787	FPGA-Based CNN for Eye Detection in an Iris Recognition at a Distance System. Electronics (Switzerland), 2023, 12, 4713.	3.1	1
1788	FPGA Hardware Implementation of Efficient Long Short-Term Memory Network Based on Construction Vector Method. IEEE Access, 2023, 11, 122357-122367.	4.2	1

#	Article	IF	Citations
1789	Multiply-and-Fire: An Event-Driven Sparse Neural Network Accelerator. Transactions on Architecture and Code Optimization, 2023, 20, 1-26.	2.0	0
1790	Hardware-Aware Evolutionary Approaches to Deep Neural Networks. Genetic and Evolutionary Computation, 2024, , 367-396.	1.0	0
1791	Mathematical Framework for Optimizing Crossbar Allocation for ReRAM-based CNN Accelerators. ACM Transactions on Design Automation of Electronic Systems, 2024, 29, 1-24.	2.6	0
1792	An Energy Efficient All-Digital Time-Domain Compute-in-Memory Macro Optimized for Binary Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2024, 71, 287-298.	5.4	0
1793	NASA-F: FPGA-Oriented Search and Acceleration for Multiplication-Reduced Hybrid Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2024, 71, 306-319.	5.4	0
1794	A Low-Latency Hardware Accelerator forÂYOLO Object Detection Algorithms. Lecture Notes in Computer Science, 2024, , 265-278.	1.3	0
1795	Assessing the Performance of an Architecture-Aware Optimization Tool for Neural Networks. , 2023, , .		0
1796	C-DNN: An Energy-Efficient Complementary Deep-Neural-Network Processor With Heterogeneous CNN/SNN Core Architecture. IEEE Journal of Solid-State Circuits, 2023, , 1-16.	5.4	0
1797	A 116 TOPS/W Spatially Unrolled Time-Domain Accelerator Utilizing Laddered-Inverter DTC for Energy-Efficient Edge Computing in 65 nm. IEEE Open Journal of Circuits and Systems, 2023, 4, 308-323.	1.9	0
1798	An Edge AI Accelerator Design Based on LRCN Model for Real-time EEG-based Emotion Detection System on the RISC-V FPGA Platform. , 2023, , .		0
1799	WRA-SS: A High-Performance Accelerator Integrating Winograd With Structured Sparsity for Convolutional Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, , 1-14.	3.1	0
1800	IPOCIM: Artificial Intelligent Architecture Design Space Exploration With Scalable Ping-Pong Computing-in-Memory Macro. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2024, 32, 256-268.	3.1	0
1801	An Evaluation and Architecture Exploration Engine for CNN Accelerators through Extensive Dataflow Analysis. , 2023, , .		0
1802	ADaMaT: Towards an Adaptive Dataflow for Maximising Throughput in Neural Network Inference. , 2023, , .		0
1803	An Energy-Efficient and Area-Efficient Depthwise Separable Convolution Accelerator with Minimal On-Chip Memory Access. , 2023, , .		0
1804	Review of Lightweight Deep Convolutional Neural Networks. Archives of Computational Methods in Engineering, 0, , .	10.2	0
1805	Implementation of the SoftMax Activation for Reconfigurable Neural Network Hardware Accelerators. Applied Sciences (Switzerland), 2023, 13, 12784.	2.5	0
1806	Versa-DNN: A Versatile Architecture Enabling High-Performance and Energy-Efficient Multi-DNN Acceleration. IEEE Transactions on Parallel and Distributed Systems, 2023, , 1-13.	5.6	0

#	Article	IF	Citations
1807	HighLight: Efficient and Flexible DNN Acceleration with Hierarchical Structured Sparsity. , 2023, , .		0
1808	Sparse-DySta: Sparsity-Aware Dynamic and Static Scheduling for Sparse Multi-DNN Workloads. , 2023, , .		0
1809	Si-Kintsugi: Towards Recovering Golden-Like Performance of Defective Many-Core Spatial Architectures for AI. , 2023, , .		0
1811	TileFlow: A Framework for Modeling Fusion Dataflow via Tree-based Analysis. , 2023, , .		0
1812	Symphony: Orchestrating Sparse and Dense Tensors with Hierarchical Heterogeneous Processing. ACM Transactions on Computer Systems, 2023, 41, 1-30.	0.8	0
1813	3DNN-Xplorer: A Machine Learning Framework for Design Space Exploration of Heterogeneous 3D DNN Accelerators. , 2023, , .		0
1814	Quantized Distillation: Optimizing Driver Activity Recognition Models for Resource-Constrained Environments. , 2023, , .		0
1815	Design of Optimized CNN for Image Processing using Verilog. , 2023, , .		0
1816	SRAMå˜ç®—ä¸€ä½“èŠ¯ç‰‡ç©¶ï¼šå•±•ä¸ŽæŒ‘æ˜. Scientia Sinica Informationis, 2023, , .	0.4	0
1817	Optical computing for neural ordinary differential equations. , 2023, , .		0
1818	DeepFlow: A Cross-Stack Pathfinding Framework for Distributed AI Systems. ACM Transactions on Design Automation of Electronic Systems, 2024, 29, 1-20.	2.6	0
1819	FM-P2L: An Algorithm Hardware Co-design of Fixed-Point MSBs with Power-of-2 LSBs in CNN Accelerators. , 2023, , .		0
1820	CNN Inference Accelerators with Adjustable Feature Map Compression Ratios. , 2023, , .		0
1821	FreFlex: A High-Performance Processor for Convolution and Attention Computations via Sparsity-Adaptive Dynamic Frequency Boosting. IEEE Journal of Solid-State Circuits, 2024, 59, 855-866.	5.4	0
1822	An Efficient Accelerator on FPGA for Large Convolution and Correlation using Winograd. , 2023, , .		0
1823	Smart vision chip. Chinese Science Bulletin, 2023, 68, 4844-4861.	0.7	1
1824	Pianissimo: A Sub-mW Class DNN Accelerator With Progressively Adjustable Bit-Precision. IEEE Access, 2023, , 1-1.	4.2	0
1825	Deep neural networks accelerators with focus on tensor processors. Microprocessors and Microsystems, 2024, 105, 105005.	2.8	0

#	Article	IF	Citations
1826	Hardware Implementation of nmODE on FPGA. , 2023, , .		0
1827	CiTST-AdderNets: Computing in Toggle Spin Torques MRAM for Energy-Efficient AdderNets. IEEE Transactions on Circuits and Systems I: Regular Papers, 2024, 71, 1130-1143.	5.4	0
1828	Application-level Validation of Accelerator Designs Using a Formal Software/Hardware Interface. ACM Transactions on Design Automation of Electronic Systems, 2024, 29, 1-25.	2.6	0
1829	Heterogeneous Chiplet Solution for Non-volatile In-memory Computing Architecture. , 2023, , .		0
1830	Path-Based Processing using In-Memory Systolic Arrays for Accelerating Data-Intensive Applications. , 2023, , .		0
1831	Multichannel meta-imagers for accelerating machine vision. Nature Nanotechnology, 2024, 19, 471-478.	31.5	3
1832	READ: Reliability-Enhanced Accelerator Dataflow Optimization Using Critical Input Pattern Reduction. , 2023, , .		0
1833	FSS: algorithm and neural network accelerator for style transfer. Science China Information Sciences, 2024, 67, .	4.3	0
1834	Real-Time FPGA Implementation of CNN-Based Distributed Fiber Optic Vibration Event Recognition Method. , 2023, , .		0
1835	Examination of the Multimodal Nature of Multi-Objective Neural Architecture Search. , 2023, , .		0
1836	Efficient CNN Hardware Architecture Based on Linear Approximation and Computation Reuse Technique. , 2023, , .		0
1837	StarSPA: Stride-Aware Sparsity Compression for Efficient CNN Acceleration. IEEE Access, 2024, 12, 10893-10909.	4.2	0
1838	Statistical Characterization of ReRAM Arrays for Analog In-Memory Computing. , 2023, , .		0
1839	MST-compression: Compressing and Accelerating Binary Neural Networks with Minimum Spanning Tree. , 2023, , .		0
1840	Evaluation Model for Current-Domain SRAM-based Computing-in-Memory Circuits. , 2023, , .		0
1841	Unlocking the resistive switching in Acacia Senegal-based electrolyte for neuromorphic computation. Journal of Materials Chemistry C, 2024, 12, 2173-2183.	5.5	0
1842	Design of The Ultra-Low-Power Driven VMM Configurations for Î¼W Scale IoT Devices. , 2023, , .		0
1843	Selective Pruning of Sparsity-Supported Energy-Efficient Accelerator for Convolutional Neural Networks. , 2023, , .		0

#	Article	IF	Citations
1844	A Energy-Efficient Re-configurable Multi-mode Convolution Neuron Network Accelerator. , 2023, , .		0
1845	A 128-channel real-time VPDNN stimulation system for a visual cortical neuroprosthesis. , 2023, , .		0
1846	Enabling Ultra-Low Power Ultrasound Imaging with Compute-in-Memory Sparse Reconstruction Accelerator. , 2023, , .		0
1847	Algorithm-System-Hardware Co-Design for Efficient 3D Deep Learning. , 2024, 02, .		0
1848	An Edge AI Accelerator of LRCN Model with RISC-V Platform for EEG-based Emotion Real-time Detection System. , 2023, , .		0
1849	Loop-Tiling Based Compiling Optimization for CNN Accelerators. , 2023, , .		0
1850	Mitigating Non-ideality Issues of Analog Computing-In-Memory in DNN-based designs. , 2023, , .		0
1851	Memory-Efficient Compression Based on Least-Squares Fitting in Convolutional Neural Network Accelerators. , 2023, , .		0
1852	An NoC-based CNN Accelerator for Edge Computing. , 2023, , .		0
1853	A Domain-Specific DMA Structure for Per-channel Processing-based CNN Accelerator. , 2023, , .		0
1854	A Reusable AI acceleration Architecture based on Matrix Multiplication for Convolutional Neural Network with Digital Signal ProcessingTasks. , 2023, , .		0
1855	A Dynamic Codec with Adaptive Quantization for Convolution Neural Network. , 2023, , .		0
1856	8T-SRAM Based Process-In-Memory (PIM) System With Current Mirror for Accurate MAC Operation. IEEE Access, 2024, 12, 24254-24261.	4.2	0
1857	FPGA Implementation of Complex-Valued Neural Network for Polar-Represented Image Classification. Sensors, 2024, 24, 897.	3.8	0
1858	Bottlenecks in Secure Adoption of Deep Neural Networks in Safety-Critical Applications. , 2023, , .		0
1859	Winols: A Large-Tiling Sparse Winograd CNN Accelerator on FPGAs. Transactions on Architecture and Code Optimization, 2024, 21, 1-24.	2.0	0
1860	Ultrahigh framerate vision chip featuring central-based edge detection processed by all-digital in-imager global-parallel processing architecture. IEICE Electronics Express, 2024, 21, 20230627-20230627.	0.8	0
1861	Compute-In-Memory Technologies for Deep Learning Acceleration. IEEE Nanotechnology Magazine, 2024, 18, 44-52.	1.3	0

#	Article	IF	Citations
1862	MiniMalloc: A Lightweight Memory Allocator for Hardware-Accelerated Machine Learning. , 2023, , .		0
1863	Explainable-DSE: An Agile and Explainable Exploration of Efficient HW/SW Codesigns of Deep Learning Accelerators Using Bottleneck Analysis. , 2023, , .		0
1864	Empowering edge devices: FPGAâ€based 16â€bit fixedâ€point accelerator with SVD for CNN on 32â€bit memoryâ€limited systems. International Journal of Circuit Theory and Applications, 0, , .	2.0	0
1865	Design of a Generic Dynamically Reconfigurable Convolutional Neural Network Accelerator with Optimal Balance. Electronics (Switzerland), 2024, 13, 761.	3.1	0
1866	Negative capacitance FET based dual-split control 6T-SRAM cell design for energy efficient and robust computing-in memory architectures. Microelectronic Engineering, 2024, 288, 112165.	2.4	0
1867	CSDSE: Apply Cooperative Search toÂSolve theÂExploration-Exploitation Dilemma ofÂDesign Space Exploration. Lecture Notes in Computer Science, 2024, , 1-23.	1.3	0
1868	Performance Impact of Architectural Parameters on Chiplet-Based IMC Accelerators. , 2023, , .		0
1869	Novel Edge AI with Power-Efficient Re-configurable LP-MAC Processing Elements. , 2023, , .		0
1870	Heterogeneous network influence maximization algorithm based on multi-scale propagation strength and repulsive force of propagation field. Knowledge-Based Systems, 2024, 291, 111580.	7.1	0
1871	Hardware implementation of memristor-based artificial neural networks. Nature Communications, 2024, 15, .	12.8	0
1872	Design of a Convolutional Neural Network Accelerator Based on On-Chip Data Reordering. Electronics (Switzerland), 2024, 13, 975.	3.1	0
1873	CUTE: A scalable CPU-centric and Ultra-utilized Tensor Engine for convolutions. Journal of Systems Architecture, 2024, 149, 103106.	4.3	0
1874	Spectral-Blaze: A High-Performance FFT-Based CNN Accelerator. Lecture Notes in Computer Science, 2024, , 222-238.	1.3	0
1875	Computing in-memory reconfigurable (accurate/approximate) adder design with negative capacitance FET 6T-SRAM for energy efficient AI edge devices. Semiconductor Science and Technology, 2024, 39, 055001.	2.0	0
1876	A methodological framework for optimizing the energy consumption of deep neural networks: a case study of a cyber threat detector. Neural Computing and Applications, 0, , .	5.6	0
1877	Hardware for Deep Learning Acceleration. Advanced Intelligent Systems, 0, , .	6.1	0