Citation Report
List of articles citing

Finite memory test response compactors for embedded test applications

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#	Paper	IF	Citations
62	Column parity and row selection (CPRS): a BIST diagnosis technique for multiple errors in multiple scan chains.		
61	A Unified Approach to Test Generation and Test Data Volume Reduction. *IEEE International Test Conference (TC)*, **2006**,		2
60	Convolutional Compactors with Variable Polynomials.		
59	Cyclic-CPRS : A Diagnosis Technique for BISTed Circuits for Nano-meter Technologies. **2007**,		
58	Test data compression and TAM design. **2007**,		
57	Fault Diagnosis With Convolutional Compactors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 1478-1494	2.5	8
56	Column Parity Row Selection (CPRS) BIST Diagnosis Technique: Modeling and Analysis. *IEEE Transactions on Computers*, **2007**, 56, 402-414	2.5	6
55	X-canceling MISR — An X-tolerant methodology for compacting output responses with unknowns using a MISR. **2007**,		41
54	Increasing Output Compaction in Presence of Unknowns Using an X-Canceling MISR with Deterministic Observation. *VLSI Test Symposium (VTS), Proceedings, IEEE*, **2008**,		14
53	Constructing Augmented Multimode Compactors. *VLSI Test Symposium (VTS), Proceedings, IEEE*, **2008**,		5
52	Improving the Test of NoC-Based SoCs with Help of Compression Schemes. **2008**,		18
51	Scan Chain Organization for Embedded Diagnosis. **2008**,		4
50	Scan chain organization for embedded diagnosis. **2008**,		1
49	Using reiterative LFSR based X-masking to increase output compression in presence of unknowns. **2008**,		0
48	Design for testability. **2009**, 97-172		1
47	A diagnosis algorithm for extreme space compaction. **2009**,		10
46	A response compactor for extended compatibility scan tree construction. **2009**,		3

45	Test Encoding for Extreme Response Compaction. **2009**,		2
44	An industrial case study for X-canceling MISR. **2009**,		5
43	Linear and nonlinear MISR operations for safety and security in automotive applications. **2009**,		1
42	Compression-aware pseudo-functional testing. **2009**,		5
41	Time-space test response compaction and diagnosis based on BCH codes. *IET Computers and Digital Techniques*, **2009**, 3, 304	0.9	
40	. **2010**,		3
39	ATE assisted test response compaction. **2010**,		0
38	BISD: Scan-based Built-In self-diagnosis. **2010**,		7
37	On Determining the Real Output Xs by SAT-Based Reasoning. **2010**,		4
36	An output compression scheme for handling X-states from over-clocked delay tests. **2010**,		13
35	FiX-compact: A new X-tolerant response compaction scheme for fixed unknown logic values. **2010**,		
34	Structural In-Field Diagnosis for Random Logic Circuits. **2011**,		10
33	Diagnostic Test of Robust Circuits. **2011**,		3
32	Trade-Offs in Test Data Compression and Deterministic X-Masking of Responses. *IEEE Transactions on Computers*, **2011**, 60, 498-507	2.5	1
31	Test Response Compaction via Output Bit Selection. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 1534-1544	2.5	12
30	Construction and Analysis of Augmented Time Compactors. *Journal of Electronic Testing: Theory and Applications (JETTA)*, **2011**, 27, 109-122	0.7	2
29	Fault diagnosis aware ATE assisted test response compaction. **2011**,		0
28	A selective X-masking for test responses in the presence of unknown values. **2011**,		1

#	Paper	IF	Citations
27	Output bit selection for test response compaction based on a single counter. **2012**,		1
26	Exploiting X-correlation in output compression via superset X-canceling. **2012**,		
25	Built-in self-diagnosis exploiting strong diagnostic windows in mixed-mode test. **2012**,		2
24	Are advanced DfT structures sufficient for preventing scan-attacks?. **2012**,		32
23	X-Canceling MISR Architectures for Output Response Compaction With Unknown Values. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1417-1427	2.5	9
22	Accurate X-Propagation for Test Applications by SAT-Based Reasoning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1908-1919	2.5	6
21	Counter-Based Output Selection for Test Response Compaction. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 152-164	2.5	5
20	Unknown Output Values of Faulty Circuits and Output Response Compaction. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 323-327	2.5	1
19	Improving Output Compaction Efficiency with High Observability Scan Chains. **2014**,		
18	MISR architectures to remove unknown values in output response compaction. **2014**,		1
17	Handling wrong mapping: A new direction towards better diagnosis with low pin convolution compressors. **2016**,		
16	Using symbolic canceling to improve diagnosis from compacted response. **2016**,		
15	Reducing control bit overhead for X-masking/X-canceling hybrid architecture via pattern partitioning. **2016**,		3
14	Enhancing Superset X -Canceling Method With Relaxed Constraints on Fault Observation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 298-308	2.5	2
13	Trimodal Scan-Based Test Paradigm. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* , **2017**, 25, 1112-1125	2.6	23
12	Full-scan LBIST with capture-per-cycle hybrid test points. **2017**,		6
11	Output compaction for high X-densities via improved input rotation compactor design. **2017**,		0
10	Mitigating Observability Loss of Toggle-Based X-Masking via Scan Chain Partitioning. *IEEE Transactions on Computers*, **2018**, 67, 1184-1192	2.5	2

#	Article		
9	Handling Unknown with Blend of Scan and Scan Compression. *Journal of Electronic Testing: Theory and Applications (JETTA)*, **2018**, 34, 135-146	0.7	2
8	On New Class of Test Points and Their Applications. **2018**,		1
7	Staggered ATPG with capture-per-cycle observation test points. **2018**,		7
6	Logic BIST With Capture-Per-Clock Hybrid Test Points. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 1028-1041	2.5	15
5	A Test Response Compression Method for Monolithic 3-D ICs Based on 3-D Haar Wavelet Transforms. *IEEE Transactions on Instrumentation and Measurement*, **2021**, 70, 1-12	5.2	
4	Digital Test Architectures. **2008**, 41-121		7
3	Test Compression. **2006**, 341-396		2
2	DFG-Projekt RealTest □Test und Zuverl□sigkeit nanoelektronischer Systeme (DFG-Project □Test and Reliability of Nano-Electronic Systems). *IT - Information Technology*, **2006**, 48, 304-311	0.4	1
1	X-Handling for Current X-Tolerant Compactors with More Unknowns and Maximal Compaction. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2009**, E92-A, 3119-3127	0.4	