Low-voltage adders for power-efficient arithmetic circu

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#	Article	IF	Citations
1	Novel design and verification of a 16 x 16-b self-repairable reconfigurable inner product processor. , 2002, , .		5
2	Physical implementation and test of energy recovery circuit. , 2003, , .		0
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5	A mutated additionâ€“subtraction unit to reduce the complexity of FFT. Applied Nanoscience (Switzerland), 2023, 13, 2935-2944.	3.1	2
6	Power and Area Efficient Multi-operand Binary Tree Adder. , 2022, , .		0