

High-density chain ferroelectric random access memory

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Citation Report

#	ARTICLE	IF	CITATIONS
1	Tunnelling-based SRAM. <i>Nanotechnology</i> , 1999, 10, 174-186.	2.6	34
2	A sub-40 ns random-access chain FRAM architecture with a 768 cell-plate-line drive. , 0, , .	4	
3	A sub-40-ns chain FRAM architecture with 7-ns cell-plate-line drive. <i>IEEE Journal of Solid-State Circuits</i> , 1999, 34, 1557-1563.	5.4	12
4	Tunneling-based SRAM. <i>Proceedings of the IEEE</i> , 1999, 87, 571-595.	21.3	116
5	Degradation of Ferroelectric Capacitors during Metal Etching and Ashing Processes. <i>Materials Research Society Symposia Proceedings</i> , 2000, 655, 284.	0.1	0
6	A 3.3-V, 4-Mb nonvolatile ferroelectric RAM with selectively driven double-pulsed plate read/write-back scheme. <i>IEEE Journal of Solid-State Circuits</i> , 2000, 35, 697-704.	5.4	18
7	A survey of circuit innovations in ferroelectric random-access memories. <i>Proceedings of the IEEE</i> , 2000, 88, 667-689.	21.3	181
8	A 76-mm ² /8-Mb chain ferroelectric memory. <i>IEEE Journal of Solid-State Circuits</i> , 2001, 36, 1713-1720.	5.4	28
9	Comparison between standard and chain-type FRAM architectures. <i>Integrated Ferroelectrics</i> , 2001, 34, 1-10.	0.7	0
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11	Advanced simulation tool for FeRAM design. <i>Integrated Ferroelectrics</i> , 2001, 40, 101-112.	0.7	6
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16	A 32-Mb chain FeRAM with segment/stitch array architecture. <i>IEEE Journal of Solid-State Circuits</i> , 2003, 38, 1911-1919.	5.4	12
17	Retention and Read Endurance Characteristics of a Ferroelectric Gate Field Effect Transistor Memory with an Intermediate Electrode. <i>Japanese Journal of Applied Physics</i> , 2004, 43, 2220-2225.	1.5	6
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21	A NEW HIGH-RELIABLE 2T/1C FeRAM CELL. Integrated Ferroelectrics, 2006, 81, 149-155.	0.7	0
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