

# Mohammad Bagher Ghaznavi-Ghousheh

## List of Publications by Year in descending order

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74  
papers

368  
citations

1305906

8  
h-index

1113639

15  
g-index

74  
all docs

74  
docs citations

74  
times ranked

385  
citing authors

#	ARTICLE	IF	CITATIONS
1	ML-Based Aging Monitoring and Lifetime Prediction of IoT Devices With Cost-Effective Embedded Tags for Edge and Cloud Operability. <i>IEEE Internet of Things Journal</i> , 2022, 9, 7433-7445.	5.5	4
2	A novel generic modulo-2 graph with full set taxonomical conversion to parallel prefix adders. <i>International Journal of Circuit Theory and Applications</i> , 2022, 50, 1143-1159.	1.3	1
3	AMPS: An Automated Mesochronous Pipeline Scheduler and Design Space Explorer for High Performance Digital Circuits. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2022, 69, 1681-1692.	3.5	2
4	A New Side-Channel Attack on Reduction of RSA-CRT Montgomery Method Based. <i>Journal of Circuits, Systems and Computers</i> , 2021, 30, 2150038.	1.0	4
5	A New Low Power Schema for Stream Processors Front-End with Power-Aware DA-Based FIR Filters by Investigation of Image Transitions Sparsity. <i>Circuits, Systems, and Signal Processing</i> , 2021, 40, 3456-3478.	1.2	0
6	Low-voltage and high-speed stand-alone multiple-input complex gates for error correction coding applications. <i>International Journal of Circuit Theory and Applications</i> , 2021, 49, 921-937.	1.3	2
7	An Ultra-Low Power Programmable Current Gain Amplifier with a Novel Current Gain Controller Structure for IoT Applications. <i>Wireless Personal Communications</i> , 2020, 114, 3577-3593.	1.8	1
8	PDP and TPD Flexible MCML and MTCML Ultralow-Power and High-Speed Structures for Wireless and Wireline Applications. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2020, 28, 1782-1795.	2.1	6
9	A DPA Attack on IOA Data-Dependent Delay Countermeasure Based on an Inherent Tempo-Spatial Data Dependency. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2019, 66, 1341-1345.	2.2	2
10	Optimistic Modeling and Simulation of Complex Hardware Platforms and Embedded Systems on Many-Core HPC Clusters. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2019, 30, 428-444.	4.0	0
11	A Low-Power CMOS Transceiver in 130Ånm for Wireless Sensor Network Applications. <i>Wireless Personal Communications</i> , 2019, 106, 1015-1039.	1.8	3
12	Design of low-voltage shallow-depth differential source coupled logic using feedback and feedforward techniques. <i>Microelectronics Journal</i> , 2019, 86, 140-149.	1.1	3
13	PSML: parallel system modeling and simulation language for electronic system level. <i>Journal of Supercomputing</i> , 2019, 75, 2691-2724.	2.4	0
14	A fully pipelined and parallel hardware architecture for real-time BRISK salient point extraction. <i>Journal of Real-Time Image Processing</i> , 2019, 16, 1859-1879.	2.2	5
15	A high-precision time-domain RRAM state control approach. <i>Microelectronics Journal</i> , 2018, 74, 94-105.	1.1	8
16	NEMR: A Nonequidistant DPA Attack-Proof of Modular Reduction in a CRT Implementation of RSA. <i>Journal of Circuits, Systems and Computers</i> , 2018, 27, 1850191.	1.0	4
17	A low-area, 43.5% PAE, 0.9 W, Class-E differential power amplifier in 2.4 GHz for IoT applications. <i>The Integration VLSI Journal</i> , 2018, 61, 178-185.	1.3	1
18	A power-performance tunable logic with adjustable threshold pseudo-dynamic building blocks and CMOS compatibility. <i>International Journal of Circuit Theory and Applications</i> , 2018, 46, 796-811.	1.3	1

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19	An output node split CMOS logic for high-performance and large capacitive-load driving scenarios. <i>Microelectronics Journal</i> , 2018, 72, 109-119.	1.1	2
20	Low-complexity and differential power analysis (DPA)-resistant two-folded power-aware Rivest-Shamir-Adleman (RSA) security schema implementation for IoT-connected devices. <i>IET Computers and Digital Techniques</i> , 2018, 12, 279-288.	0.9	11
21	Two 3.9 ppm/°C curvature-corrected band gap voltage references with fast and low-power start ups. <i>International Journal of Electronics Letters</i> , 2017, 5, 45-61.	0.7	1
22	The Parvicursor infrastructure to facilitate the design of Grid and Cloud computing systems. <i>Computing (Vienna/New York)</i> , 2017, 99, 979-1006.	3.2	3
23	Design and analysis of a high speed double-tail comparator with isomorphic latch-preamplifier pairs and tail bootstrapping. <i>Analog Integrated Circuits and Signal Processing</i> , 2017, 93, 507-521.	0.9	6
24	MTCML: Analysis, design and optimization of an alternative shallow-depth multiple-tail current mode logic. <i>Microelectronics Journal</i> , 2017, 67, 57-70.	1.1	7
25	A Novel Fully Differential CMOS Class-E Power Amplifier with Higher Output Power and Efficiency for IoT Application. <i>Wireless Personal Communications</i> , 2017, 97, 3203-3213.	1.8	8
26	A Process-Independent and Highly Linear DCO for Crowded Heterogeneous IoT Devices in 65-nm CMOS. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2017, 25, 3369-3379.	2.1	10
27	Memristor based circuit design using charge and attached capacitor. <i>Microelectronics Journal</i> , 2016, 55, 53-63.	1.1	5
28	A 35.6dB, 43.3% PAE class E differential power amplifier in 2.4GHz with cross coupling neutralization for IoT applications. , 2016, , .		9
29	A 98.1% CE, 100mA MLC multi-reference output all digital LDO with fast settling and digital self calibration for DVFS and multi-VDD applications. <i>Analog Integrated Circuits and Signal Processing</i> , 2016, 89, 437-450.	0.9	3
30	1.45GHz differential dual band ring based digitally-controlled oscillator with a reconfigurable delay element in 0.18µm CMOS process. <i>Analog Integrated Circuits and Signal Processing</i> , 2016, 89, 461-467.	0.9	6
31	A differential dual delay mode Schmitt Trigger with 449ps delay gap by reconfiguring with one bit and FVF current source. , 2016, , .		2
32	A 2.7 to 4.6 GHz multi-phase high resolution and wide tuning range digitally-controlled oscillator in CMOS 65nm. , 2016, , .		6
33	A 3.48ps jitter @ 1.45GHz fully differential dual band DCO with a new reconfigurable delay cell. , 2016, , .		2
34	Design and implementation of a power and area optimized reconfigurable superset parallel prefix adder. , 2016, , .		3
35	Hardware architecture for projective model calculation and false match refining using random sample consensus algorithm. <i>Journal of Electronic Imaging</i> , 2016, 25, 063014.	0.5	2
36	Two Efficient Dual-Band and Wide-Band Low-Power DCO Designs Using Current Starving Gates, DCV and Reconfigurable Schmitt Triggers in 180nm. <i>Circuits, Systems, and Signal Processing</i> , 2016, 35, 1481-1505.	1.2	8

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37	A new Chua's circuit with monolithic Chua's diode and its use for efficient true random number generation in CMOS 180nm. Analog Integrated Circuits and Signal Processing, 2015, 82, 719-731.	0.9	11
38	A 14.8ps jitter low-power dual band all digital PLL with reconfigurable DCO and time-interlined multiplexers. Analog Integrated Circuits and Signal Processing, 2015, 82, 381-392.	0.9	7
39	Workload and temperature dependent evaluation of BTI-induced lifetime degradation in digital circuits. Microelectronics Reliability, 2015, 55, 1152-1162.	0.9	5
40	Energy-efficient secure distributed storage in mobile cloud computing. , 2015, , .		2
41	A new parallel prefix adder structure with efficient critical delay path and graded bits efficiency in CMOS 90nm technology. , 2015, , .		4
42	A power efficient multi-level output all digital LDO with fast settling time and built in self calibration for DVFS and multi-VDD applications. , 2015, , .		3
43	A new secure Internet voting protocol using Java Card 3 technology and Java information flow concept. Security and Communication Networks, 2015, 8, 261-283.	1.0	4
44	CSAM: A clock skew-aware aging mitigation technique. Microelectronics Reliability, 2015, 55, 282-290.	0.9	4
45	TSSL: improving SSL/TLS protocol by trust model. Security and Communication Networks, 2015, 8, 1659-1671.	1.0	3
46	A low-power dual band all digital PLL with precision dual mode DCO and digital linearization control circuits. , 2014, , .		1
47	A 3.9ppm/°C curvature-corrected bandgap voltage reference. , 2014, , .		1
48	A 68.8ps jitter, 1.685mw band-selective reconfigurable DCO design for overlapped and non-overlapped applications in 180nm. , 2014, , .		0
49	VLSI implementation of star detection and centroid calculation algorithms for star tracking applications. Journal of Real-Time Image Processing, 2014, 9, 127-140.	2.2	12
50	Personalized recommendation of learning material using sequential pattern mining and attribute based collaborative filtering. Education and Information Technologies, 2014, 19, 713-735.	3.5	63
51	A New Low-Power Architecture Design for Distributed Arithmetic Unit in FIR Filter Implementation. Circuits, Systems, and Signal Processing, 2014, 33, 1245-1259.	1.2	6
52	Design and implementation of a novel secure internet voting protocol using Java Card 3 technology. International Journal of Business Information Systems, 2014, 17, 414.	0.2	1
53	Creating a novel semantic video search engine through enrichment textual and temporal features of subtitled YouTube media fragments. , 2013, , .		7
54	Attribute-based collaborative filtering using genetic algorithm and weighted C-means algorithm. International Journal of Business Information Systems, 2013, 13, 265.	0.2	9

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55	An effective recommendation framework for personal learning environments using a learner preference tree and a GA. IEEE Transactions on Learning Technologies, 2013, 6, 350-363.	2.2	34
56	Self-impact of NBTI effect on the degradation rate of threshold voltage in PMOS transistors. , 2013, , .		1
57	A 2-bit/step SAR ADC structure with one radix-4 DAC. IEICE Electronics Express, 2012, 9, 840-848.	0.3	0
58	The xDotGrid native, cross-platform, high-performance xDFS file transfer framework. Computers and Electrical Engineering, 2012, 38, 1409-1432.	3.0	1
59	A high performance, race eliminated, two phase nonoverlapping clocked All-N-Logic for both strong and subthreshold designs. , 2012, , .		2
60	Two phase nonoverlapping clocked All-N-Logic in subthreshold region with 49fJ power delay product. , 2012, , .		0
61	A low-power low-area architecture design for distributed arithmetic (DA) unit. , 2012, , .		7
62	Improvement of timing specifications in second order electronic systems using programmable CMOS Posicast pulse shapers. , 2012, , .		1
63	Low rate DOS traceback based on sum of flows. , 2012, , .		4
64	PABEM: A new power-aware adaptive bus encoding method using Huffman algorithm. , 2011, , .		3
65	Performance improvement of differential static CMOS logic family. , 2011, , .		1
66	A new low-power, low-area, parallel prefix Sklansky adder with reduced inter-stage connections complexity. , 2011, , .		3
67	An ultra low-power digitally controlled oscillator using novel Schmitt-trigger based hysteresis delay cells. IEICE Electronics Express, 2011, 8, 589-595.	0.3	4
68	An ultra low power and low complexity all digital PLL with a high resolution digitally controlled oscillator. IEICE Electronics Express, 2011, 8, 1801-1807.	0.3	7
69	DotDFS: A Grid-based high-throughput file transfer system. Parallel Computing, 2011, 37, 114-136.	1.3	1
70	A New CMOS Posicast Pre-shaper for Vibration Reduction of CMOS Op-Amps. , 2010, , .		2
71	A novel method for oscillation canceling of CMOS operational amplifiers using Posicast. , 2010, , .		2
72	Oscillation controlled electronic systems design using Posicast-based pulse pre-shaping. , 2009, , .		5

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73	A Multi-Gb/s Parallel String Matching Engine for Intrusion Detection Systems. Communications in Computer and Information Science, 2008, , 847-851.	0.4	4
74	A power-performance partitioning approach for low-power DA-based FIR filter design with emphasis on datapath and controller. International Journal of Circuit Theory and Applications, 0, , .	1.3	2