Mohammad Bagher Ghaznavi-Ghoushcl

List of Publications by Year
in descending order

74 papers	368 citations	1163117 8 h-index	996975 15 g-index
74 all docs	74 docs citations	74 times ranked	350 citing authors

#	Article	IF	Citations
1	Personalized recommendation of learning material using sequential pattern mining and attribute based collaborative filtering. Education and Information Technologies, 2014, 19, 713-735.	5.7	63
2	An effective recommendation framework for personal learning environments using a learner preference tree and a GA. IEEE Transactions on Learning Technologies, 2013, 6, 350-363.	3.2	34
3	VLSI implementation of star detection and centroid calculation algorithms for star tracking applications. Journal of Real-Time Image Processing, 2014, 9, 127-140.	3.5	12
4	A new Chuaâ€™s circuit with monolithic Chuaâ€™s diode and its use for efficient true random number generation in CMOS 180Ânm. Analog Integrated Circuits and Signal Processing, 2015, 82, 719-731.	1.4	11
5	Lowâ€complexity and differential power analysis (DPA)â€resistant twoâ€folded powerâ€aware Rivestâ€“Shamirâ€“Adleman (RSA) security schema implementation for IoTâ€connected devices. IET Computers and Digital Techniques, 2018, 12, 279-288.	1.2	11
6	A Process-Independent and Highly Linear DCO for Crowded Heterogeneous IoT Devices in 65-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3369-3379.	3.1	10
7	Attribute-based collaborative filtering using genetic algorithm and weighted C-means algorithm. International Journal of Business Information Systems, 2013, 13, 265.	0.2	9
8	A 35.6dB, 43.3% PAE class E differential power amplifier in 2.4GHz with cross coupling neutralization for IoT applications. , 2016, , .		9
9	Two Efficient Dual-Band and Wide-Band Low-Power DCO Designs Using Current Starving Gates, DCV and Reconfigurable Schmitt Triggers in 180Ânm. Circuits, Systems, and Signal Processing, 2016, 35, 1481-1505.	2.0	8
10	A Novel Fully Differential CMOS Class-E Power Amplifier with Higher Output Power and Efficiency for IoT Application. Wireless Personal Communications, 2017, 97, 3203-3213.	2.7	8
11	A high-precision time-domain RRAM state control approach. Microelectronics Journal, 2018, 74, 94-105.	2.0	8
12	An ultra low power and low complexity all digital PLL with a high resolution digitally controlled oscillator. IEICE Electronics Express, 2011, 8, 1801-1807.	0.8	7
13	A low-power low-area architecture design for distributed arithmetic (DA) unit. , 2012, , .		7
14	Creating a novel semantic video search engine through enrichment textual and temporal features of subtitled YouTube media fragments. , 2013, , .		7
15	A 14.8Âps jitter low-power dual band all digital PLL with reconfigurable DCO and time-interlined multiplexers. Analog Integrated Circuits and Signal Processing, 2015, 82, 381-392.	1.4	7
16	MTCML: Analysis, design and optimization of an alternative shallow-depth multiple-tail current mode logic. Microelectronics Journal, 2017, 67, 57-70.	2.0	7
17	A New Low-Power Architecture Design for Distributed Arithmetic Unit in FIR Filter Implementation. Circuits, Systems, and Signal Processing, 2014, 33, 1245-1259.	2.0	6
18	1.45ÂGHz differential dual band ring based digitally-controlled oscillator with a reconfigurable delay element in 0.18ÂÎ¼m CMOS process. Analog Integrated Circuits and Signal Processing, 2016, 89, 461-467.	1.4	6

#	Article	IF	Citations
19	A 2.7 to 4.6 GHz multi-phase high resolution and wide tuning range digitally-controlled oscillator in CMOS 65nm. , 2016, , .		6
20	Design and analysis of a high speed double-tail comparator with isomorphic latch-preamplifier pairs and tail bootstrapping. Analog Integrated Circuits and Signal Processing, 2017, 93, 507-521.	1.4	6
21	PDP and TPD Flexible MCML and MTCML Ultralow-Power and High-Speed Structures for Wireless and Wireline Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1782-1795.	3.1	6
22	Oscillation controlled electronic systems design using Posicast-based pulse pre-shaping. , 2009, , .		5
23	Workload and temperature dependent evaluation of BTI-induced lifetime degradation in digital circuits. Microelectronics Reliability, 2015, 55, 1152-1162.	1.7	5
24	Memristor based circuit design using charge and attached capacitor. Microelectronics Journal, 2016, 55, 53-63.	2.0	5
25	A fully pipelined and parallel hardware architecture for real-time BRISK salient point extraction. Journal of Real-Time Image Processing, 2019, 16, 1859-1879.	3.5	5
26	A Multi-Gb/s Parallel String Matching Engine for Intrusion Detection Systems. Communications in Computer and Information Science, 2008, , 847-851.	0.5	4
27	An ultra low-power digitally controlled oscillator using novel Schmitt-trigger based hysteresis delay cells. IEICE Electronics Express, 2011, 8, 589-595.	0.8	4
28	Low rate DOS traceback based on sum of flows. , 2012, , .		4
29	A new parallel prefix adder structure with efficient critical delay path and gradded bits efficiency in CMOS 90nm technology. , 2015, , .		4
30	A new secure Internet voting protocol using Java Card 3 technology and Java information flow concept. Security and Communication Networks, 2015, 8, 261-283.	1.5	4
31	CSAM: A clock skew-aware aging mitigation technique. Microelectronics Reliability, 2015, 55, 282-290.	1.7	4
32	NEMR: A Nonequidistant DPA Attack-Proof of Modular Reduction in a CRT Implementation of RSA. Journal of Circuits, Systems and Computers, 2018, 27, 1850191.	1.5	4
33	A New Side-Channel Attack on Reduction of RSA-CRT Montgomery Method Based. Journal of Circuits, Systems and Computers, 2021, 30, 2150038.	1.5	4
34	ML-Based Aging Monitoring and Lifetime Prediction of IoT Devices With Cost-Effective Embedded Tags for Edge and Cloud Operability. IEEE Internet of Things Journal, 2022, 9, 7433-7445.	8.7	4
35	PABEM: A new power-aware adaptive bus encoding method using Huffman algorithm. , 2011, , .		3
36	A new low-power, low-area, parallel prefix Sklansky adder with reduced inter-stage connections complexity. , 2011, , .		3

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37	A power efficient multi-level output all digital LDO with fast settling time and built in self calibration for DVFS and multi-VDD applications. , 2015, , .		3
38	TSSL: improving SSL/TLS protocol by trust model. Security and Communication Networks, 2015, 8, 1659-1671.	1.5	3
39	A 98.1Â% CE, 100ÂmA MLC multi-reference output all digital LDO with fast settling and digital self calibration for DVFS and multi-VDD applications. Analog Integrated Circuits and Signal Processing, 2016, 89, 437-450.	1.4	3
40	Design and implementation of a power and area optimized reconfigurable superset parallel prefix adder. , 2016, , .		3
41	The Parvicursor infrastructure to facilitate the design of Grid and Cloud computing systems. Computing (Vienna/New York), 2017, 99, 979-1006.	4.8	3
42	A Low-Power CMOS Transceiver in 130Ânm for Wireless Sensor Network Applications. Wireless Personal Communications, 2019, 106, 1015-1039.	2.7	3
43	Design of low-voltage shallow-depth differential source coupled logic using feedback and feedforward techniques. Microelectronics Journal, 2019, 86, 140-149.	2.0	3
44	A New CMOS Posicast Pre-shaper for Vibration Reduction of CMOS Op-Amps. , 2010, , .		2
45	A novel method for oscillation canceling of CMOS opeational amplifires using Posicast. , 2010, , .		2
46	A high performance, race eliminated, two phase nonoverlapping clocked All-N-Logic for both strong and subthreshold designs. , 2012, , .		2
47	Energy-efficient secure distributed storage in mobile cloud computing. , 2015, , .		2
48	A differential dual delay mode Schmitt Trigger with 449ps delay gap by reconfiguring with one bit and FVF current source. , 2016, , .		2
49	A 3.48ps jitter @ 1.45GHz fully differential dual band DCO with a new reconfigurable delay cell. , 2016, , .		2
50	Hardware architecture for projective model calculation and false match refining using random sample consensus algorithm. Journal of Electronic Imaging, 2016, 25, 063014.	0.9	2
51	An output node split CMOS logic for high-performance and large capacitive-load driving scenarios. Microelectronics Journal, 2018, 72, 109-119.	2.0	2
52	A DPA Attack on IOA Data-Dependent Delay Countermeasure Based on an Inherent Tempo-Spatial Data Dependency. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1341-1345.	3.0	2
53	Lowâ€voltage and highâ€speed standâ€alone multipleâ€input complex gates for error correction coding applications. International Journal of Circuit Theory and Applications, 2021, 49, 921-937.	2.0	2
54	A powerâ€“performance partitioning approach for lowâ€power DAâ€based FIR filter design with emphasis on datapath and controller. International Journal of Circuit Theory and Applications, 0, , .	2.0	2

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55	AMPS: An Automated Mesochronous Pipeline Scheduler and Design Space Explorer for High Performance Digital Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1681-1692.	5.4	2
56	Performance improvement of differential static CMOS logic family. , 2011, , .		1
57	DotDFS: A Grid-based high-throughput file transfer system. Parallel Computing, 2011, 37, 114-136.	2.1	1
58	The xDotGrid native, cross-platform, high-performance xDFS file transfer framework. Computers and Electrical Engineering, 2012, 38, 1409-1432.	4.8	1
59	Improvement of timing specifications in second order electronic systems using programmable CMOS Posicast pulse shapers. , 2012, , .		1
60	Self-impact of NBTI effect on the degradation rate of threshold voltage in PMOS transistors. , 2013, , .		1
61	A low-power dual band all digital PLL with precision dual mode DCO and digital linearization control circuits. , 2014, , .		1
62	A 3.9ppm/°C curvature-corrected bandgap voltage reference. , 2014, , .		1
63	Design and implementation of a novel secure internet voting protocol using Java Card 3 technology. International Journal of Business Information Systems, 2014, 17, 414.	0.2	1
64	Two 3.9 ppm/Â°C curvature-corrected band gap voltage references with fast and low-power start ups. International Journal of Electronics Letters, 2017, 5, 45-61.	1.2	1
65	A low-area, 43.5% PAE, 0.9 W, Class-E differential power amplifier in 2.4 GHz for IoT applications. The Integration VLSI Journal, 2018, 61, 178-185.	2.1	1
66	A powerâ€performance tunable logic with adjustable threshold pseudoâ€dynamic building blocks and <scp>CMOS</scp> compatibility. International Journal of Circuit Theory and Applications, 2018, 46, 796-811.	2.0	1
67	An Ultra-Low Power Programmable Current Gain Amplifier with a Novel Current Gain Controller Structure for IoT Applications. Wireless Personal Communications, 2020, 114, 3577-3593.	2.7	1
68	A novel generic moduloâ€2 graph with full set taxonomical conversion to parallel prefix adders. International Journal of Circuit Theory and Applications, 2022, 50, 1143-1159.	2.0	1
69	A 2-bit/step SAR ADC structure with one radix-4 DAC. IEICE Electronics Express, 2012, 9, 840-848.	0.8	0
70	Two phase nonoverlapping clocked All-N-Logic in subthreshold region with 49fJ power delay product. , 2012, , .		0
71	A 68.8ps jitter, 1.685mw band-selective reconfigurable DCO design for overlapped and non-overlapped applications in 180nm. , 2014, , .		0
72	Optimistic Modeling and Simulation of Complex Hardware Platforms and Embedded Systems on Many-Core HPC Clusters. IEEE Transactions on Parallel and Distributed Systems, 2019, 30, 428-444.	5.6	0

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73	PSML: parallel system modeling and simulation language for electronic system level. Journal of Supercomputing, 2019, 75, 2691-2724.	3.6	0
74	A New Low Power Schema for Stream Processors Front-End with Power-Aware DA-Based FIR Filters by Investigation of Image Transitions Sparsity. Circuits, Systems, and Signal Processing, 2021, 40, 3456-3478.	2.0	0