

Le Ye

List of Publications by Year in descending order

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#	ARTICLE	IF	CITATIONS
1	A 4-1/4W Bandwidth/Power Scalable Delta-Sigma Modulator Based on Swing-Enhanced Floating Inverter Amplifiers. IEEE Journal of Solid-State Circuits, 2022, 57, 709-718.	5.4	9
2	A 148-nW Reconfigurable Event-Driven Intelligent Wake-Up System for AIoT Nodes Using an Asynchronous Pulse-Based Feature Extractor and a Convolutional Neural Network. IEEE Journal of Solid-State Circuits, 2021, 56, 3274-3288.	5.4	18
3	Ultra-Low-Power and Performance-Improved Logic Circuit Using Hybrid TFET-MOSFET Standard Cells Topologies and Optimized Digital Front-End Process. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1160-1170.	5.4	12
4	Re-Assessment of Steep-Slope Device Design From a Circuit-Level Perspective Using Novel Evaluation Criteria and Model-Less Method. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1624-1635.	5.4	1
5	A 94.1 dB DR 4.1 nW/Hz Bandwidth/Power Scalable DTDSM for IoT Sensing Applications Based on Swing-Enhanced Floating Inverter Amplifiers. , 2021, , .		11
6	A Software-Defined Always-On System With 57-75-nW Wake-Up Function Using Asynchronous Clock-Free Pipelined Event-Driven Architecture and Time-Shielding Level-Crossing ADC. IEEE Journal of Solid-State Circuits, 2021, 56, 2804-2816.	5.4	12
7	The Challenges and Emerging Technologies for Low-Power Artificial Intelligence IoT Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4821-4834.	5.4	24
8	Energy-Efficient CMOS Humidity Sensors Using Adaptive Range-Shift Zoom CDC and Power-Aware Floating Inverter Amplifier Array. IEEE Journal of Solid-State Circuits, 2021, 56, 3560-3572.	5.4	11
9	Challenges and Solutions of the TFET Circuit Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4918-4931.	5.4	19
10	2.4-GHz 16-QAM Passive Backscatter Transmitter for Wireless Self-Power Chips in IoT. , 2020, , .		4
11	20.2 A 57nW Software-Defined Always-On Wake-Up Chip for IoT Devices with Asynchronous Pipelined Event-Driven Architecture and Time-Shielding Level-Crossing ADC. , 2020, , .		24
12	Ultra-Low Power Hybrid TFET-MOSFET Topologies for Standard Logic Cells with Improved Comprehensive Performance. , 2019, , .		11
13	Combinational Access Tunnel FET SRAM for Ultra-Low Power Applications. , 2018, , .		10
14	Benchmarking TFET from a circuit level perspective: Applications and guideline. , 2017, , .		11
15	Comprehensive performance re-assessment of TFETs with a novel design by gate and source engineering from device/circuit perspective. , 2014, , .		40