

Saibal Mukhopadhyay

List of Publications by Year in Descending Order

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Version: 2024-04-26

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

126
papers

1,404
citations

21
h-index

32
g-index

144
ext. papers

1,861
ext. citations

3.4
avg, IF

5.07
L-index

#	Paper	IF	Citations
126	MONETA: A Processing-In-Memory-Based Hardware Platform for the Hybrid Convolutional Spiking Neural Network With Online Learning.. <i>Frontiers in Neuroscience</i> , 2022 , 16, 775457	5.1	0
125	Characterization of Generalizability of Spike Timing Dependent Plasticity Trained Spiking Neural Networks. <i>Frontiers in Neuroscience</i> , 2021 , 15, 695357	5.1	1
124	Adaptive Camera Platform Using Deep Learning-Based Early Warning of Task Failures. <i>IEEE Sensors Journal</i> , 2021 , 21, 13794-13804	4	0
123	Characterization of Drain Current Variations in FeFETs for PIM-based DNN Accelerators 2021 ,		3
122	Neural Identification for Control. <i>IEEE Robotics and Automation Letters</i> , 2021 , 6, 4648-4655	4.2	1
121	MAHASIM: Machine-Learning Hardware Acceleration Using a Software-Defined Intelligent Memory System. <i>Journal of Signal Processing Systems</i> , 2021 , 93, 659-675	1.4	1
120	Robust Processing-In-Memory with Multi-bit ReRAM using Hessian-driven Mixed-Precision Computation. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2021 , 1-1	2.5	0
119	Chiplet/Interposer Co-Design for Power Delivery Network Optimization in Heterogeneous 2.5D ICs. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2021 , 1-1	1.7	1
118	Task-driven RGB-Lidar Fusion for Object Tracking in Resource-Efficient Autonomous System. <i>IEEE Transactions on Intelligent Vehicles</i> , 2021 , 1-1	5	3
117	Reliable Edge Intelligence in Unreliable Environment 2021 ,		2
116	SPEED: Spiking Neural Network With Event-Driven Unsupervised Learning and Near-Real-Time Inference for Event-Based Vision. <i>IEEE Sensors Journal</i> , 2021 , 21, 20578-20588	4	0
115	ScieNet: Deep learning with spike-assisted contextual information extraction. <i>Pattern Recognition</i> , 2021 , 118, 108002	7.7	3
114	Physics-incorporated convolutional recurrent neural networks for source identification and forecasting of dynamical systems. <i>Neural Networks</i> , 2021 , 144, 359-371	9.1	1
113	Machine Learning in Wavelet Domain for Electromagnetic Emission Based Malware Analysis. <i>IEEE Transactions on Information Forensics and Security</i> , 2021 , 1-1	8	2
112	A Deep Learning Approach for Predicting Spatiotemporal Dynamics From Sparsely Observed Data. <i>IEEE Access</i> , 2021 , 9, 64200-64210	3.5	0
111	A quantum Hopfield associative memory implemented on an actual quantum processor. <i>Scientific Reports</i> , 2021 , 11, 23391	4.9	1
110	Effect of Process Variations in Digital Pixel Circuits on the Accuracy of DNN based Smart Sensor 2020 ,		2

109	An Inductive Voltage Regulator With Overdrive Tracking Across Input Voltage in Cascoded Power Stage. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2020 , 67, 3083-3087	3.5	
108	Multispectral Information Fusion With Reinforcement Learning for Object Tracking in IoT Edge Devices. <i>IEEE Sensors Journal</i> , 2020 , 20, 4333-4344	4	4
107	A Fully Synthesized Integrated Buck Regulator with Auto-generated GDS-II in 65nm CMOS Process 2020 ,		1
106	Algorithm-Circuit Cross-layer Control for Digital Pixel Image Sensors 2020 ,		1
105	A Digital Low-Dropout Regulator With Autotuned PID Compensator and Dynamic Gain Control for Improved Transient Performance Under Process Variations and Aging. <i>IEEE Transactions on Power Electronics</i> , 2020 , 35, 3242-3253	7.2	8
104	SAFE-DNN: A Deep Neural Network With Spike Assisted Feature Extraction For Noise Robust Inference 2020 ,		2
103	Processing-In-Memory-Based On-Chip Learning With Spike-Time-Dependent Plasticity in 65-nm CMOS. <i>IEEE Solid-State Circuits Letters</i> , 2020 , 3, 278-281	2	2
102	Securing IoT Devices using Dynamic Power Management: Machine Learning Approach. <i>IEEE Internet of Things Journal</i> , 2020 , 1-1	10.7	1
101	A Flexible Precision Multi-Format In-Memory Vector Matrix Multiplication Engine in 65 nm CMOS With RF Machine Learning Support. <i>IEEE Solid-State Circuits Letters</i> , 2020 , 3, 450-453	2	1
100	Attention-Based Activation Pruning to Reduce Data Movement in Real-Time AI: A Case-Study on Local Motion Planning in Autonomous Vehicles. <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , 2020 , 10, 306-319	5.2	6
99	Architecture, Chip, and Package Codesign Flow for Interposer-Based 2.5-D Chiplet Integration Enabling Heterogeneous IP Reuse. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2020 , 28, 2424-2437	2.6	7
98	Design Flow for Active Interposer-Based 2.5-D ICs and Study of RISC-V Architecture With Secure NoC. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2020 , 10, 2047-2060	1.7	2
97	A Heterogeneous Spiking Neural Network for Unsupervised Learning of Spatiotemporal Patterns. <i>Frontiers in Neuroscience</i> , 2020 , 14, 615756	5.1	3
96	Design of Reliable DNN Accelerator with Un-reliable ReRAM 2019 ,		39
95	RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs 2019 ,		4
94	Fast and Low-Precision Learning in GPU-Accelerated Spiking Neural Network 2019 ,		7
93	Autotuning of Integrated Inductive Voltage Regulator Using On-Chip Delay Sensor to Tolerate Process and Passive Variations. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2019 , 27, 1768-1778	2.6	2
92	Multigated Carbon Nanotube Field Effect Transistors-Based Physically Unclonable Functions As Security Keys. <i>IEEE Internet of Things Journal</i> , 2019 , 6, 325-334	10.7	5

91	Energy Efficient and Side-Channel Secure Cryptographic Hardware for IoT-Edge Nodes. <i>IEEE Internet of Things Journal</i> , 2019 , 6, 421-434	10.7	24
90	CAMEL: An Adaptive Camera With Embedded Machine Learning-Based Sensor Parameter Control. <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , 2019 , 9, 498-508	5.2	5
89	On the Effect of NBTI Induced Aging of Power Stage on the Transient Performance of On-Chip Voltage Regulators 2019 ,		1
88	A Ferroelectric FET-Based Processing-in-Memory Architecture for DNN Acceleration. <i>IEEE Journal on Exploratory Solid-State Computational Devices and Circuits</i> , 2019 , 5, 113-122	2.4	20
87	Application Inference using Machine Learning based Side Channel Analysis 2019 ,		4
86	Mixture of Pre-processing Experts Model for Noise Robust Deep Learning on Resource Constrained Platforms 2019 ,		5
85	Improving Robustness of ReRAM-based Spiking Neural Network Accelerator with Stochastic Spike-timing-dependent-plasticity 2019 ,		6
84	Improved Power/EM Side-Channel Attack Resistance of 128-Bit AES Engines With Random Fast Voltage Dithering. <i>IEEE Journal of Solid-State Circuits</i> , 2019 , 54, 569-583	5.5	25
83	Design and Analysis of a Neural Network Inference Engine Based on Adaptive Weight Compression. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2019 , 38, 109-121	2.5	8
82	Exploiting on-chip power management for side-channel security 2018 ,		3
81	3-D Stacked Image Sensor With Deep Neural Network Computation. <i>IEEE Sensors Journal</i> , 2018 , 18, 4187-4199	17	
80	DeepTrain: A Programmable Embedded Platform for Training Deep Neural Networks. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018 , 37, 2360-2370	2.5	14
79	Reverse Power Delivery Network for Wireless Power Transfer. <i>IEEE Microwave and Wireless Components Letters</i> , 2018 , 28, 624-626	2.6	1
78	3D Stacked High Throughput Pixel Parallel Image Sensor with Integrated ReRAM Based Neural Accelerator 2018 ,		5
77	A ferroelectric FET based power-efficient architecture for data-intensive computing 2018 ,		13
76	An Unsupervised Anomalous Event Detection Framework with Class Aware Source Separation 2018 ,		4
75	An Energy-Quality Scalable Wireless Image Sensor Node for Object-Based Video Surveillance. <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , 2018 , 8, 591-602	5.2	2
74	Reducing Power Side-Channel Information Leakage of AES Engines Using Fully Integrated Inductive Voltage Regulator. <i>IEEE Journal of Solid-State Circuits</i> , 2018 , 53, 2399-2414	5.5	35

73	Accelerating biophysical neural network simulation with region of interest based approximation 2018,		2
72	Performance based tuning of an inductive integrated voltage regulator driving a digital core against process and passive variations 2018,		2
71	ReRAM-Based Processing-in-Memory Architecture for Recurrent Neural Network Acceleration. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2018 , 26, 2781-2794	2.6	44
70	A Power-Aware Digital Multilayer Perceptron Accelerator with On-Chip Training Based on Approximate Computing. <i>IEEE Transactions on Emerging Topics in Computing</i> , 2017 , 5, 164-178	4.1	21
69	Adaptive weight compression for memory-efficient neural networks 2017,		11
68	An All-Digital Fully Integrated Inductive Buck Regulator With A 250-MHz Multi-Sampled Compensator and a Lightweight Auto-Tuner in 130-nm CMOS. <i>IEEE Journal of Solid-State Circuits</i> , 2017 , 52, 1825-1835	5.5	21
67	Active Fluidic Cooling on Energy Constrained System-on-Chip Systems. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2017 , 7, 1813-1822	1.7	3
66	Clock Data Compensation Aware Digital Circuits Design for Voltage Margin Reduction. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2017 , 64, 2401-2413	3.9	0
65	A Single-Chip Image Sensor Node With Energy Harvesting From a CMOS Pixel Array. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2017 , 64, 2295-2307	3.9	8
64	ReRAM Crossbar based Recurrent Neural Network for human activity detection 2016,		13
63	Design, Characterization, and Application of a Field-Programmable Thermal Emulation Platform. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2016 , 6, 1330-1339	1.7	0
62	Amdahl's law for lifetime reliability scaling in heterogeneous multicore processors 2016,		3
61	Impact of Heterogeneous Technology Integration on the Power, Performance, and Quality of a 3D Image Sensor. <i>IEEE Transactions on Multi-Scale Computing Systems</i> , 2016 , 2, 61-67		1
60	(Invited paper) energy delivery for self-powered IoT devices 2016,		2
59	Thermally Adaptive Cache Access Mechanisms for 3D Many-Core Architectures. <i>IEEE Computer Architecture Letters</i> , 2016 , 15, 129-132	1.8	3
58	Partitioning Methods for Interface Circuit of Heterogeneous 3-D-ICs Under Process Variation. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2016 , 24, 1626-1635	2.6	2
57	A 190 nA Bias Current 10 mV Input Multistage Boost Regulator With Intermediate-Node Control to Supply RF Blocks in Self-Powered Wireless Sensors. <i>IEEE Transactions on Power Electronics</i> , 2016 , 31, 1322-1333	7.2	10
56	Neurocube. <i>Computer Architecture News</i> , 2016 , 44, 380-392		140

55	Reliability-performance tradeoffs between 2.5D and 3D-stacked DRAM processors 2016 ,		2
54	Neurocube: A Programmable Digital Neuromorphic Architecture with High-Density 3D Memory 2016 ,		77
53	A Memory-Based Logic Block With Optimized-for-Read SRAM for Energy-Efficient Reconfigurable Computing Fabric. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2015 , 62, 593-597	3.5	6
52	Post-Silicon Estimation of Spatiotemporal Temperature Variations Using MIMO Thermal Filters. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2015 , 5, 650-660	1.7	2
51	On the Impact of Energy-Accuracy Tradeoff in a Digital Cellular Neural Network for Image Processing. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2015 , 34, 1070-1081 ¹⁵	2.5	15
50	On-Chip Power Generation Using Ultrathin Thermoelectric Generators. <i>Journal of Electronic Packaging, Transactions of the ASME</i> , 2015 , 137,	2	6
49	Near Data Processing 2015 ,		14
48	Optimization of FinFET-based circuits using a dual gate pitch technique 2015 ,		2
47	Experimental characterization of in-package microfluidic cooling on a System-on-Chip 2015 ,		3
46	A power-aware digital feedforward neural network platform with backpropagation driven approximate synapses 2015 ,		21
45	KitFox: Multiphysics Libraries for Integrated Power, Thermal, and Reliability Simulations of Multicore Microarchitecture. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2015 , 5, 1590-1601	1.7	6
44	Negative Gate Transconductance in Gate/Source Overlapped Heterojunction Tunnel FET and Application to Single Transistor Phase Encoder. <i>IEEE Electron Device Letters</i> , 2015 , 36, 201-203	4.4	8
43	A Simulation Study of Oxygen Vacancy-Induced Variability in HfO_2 /Metal Gated SOI FinFET. <i>IEEE Transactions on Electron Devices</i> , 2014 , 61, 1262-1269	2.9	16
42	Resilient Pipeline Under Supply Noise With Programmable Time Borrowing and Delayed Clock Gating. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2014 , 61, 173-177	3.5	5
41	Control Principles and On-Chip Circuits for Active Cooling Using Integrated Superlattice-Based Thin-Film Thermoelectric Devices. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2014 , 22, 1909-1919	2.6	3
40	Post-Silicon Characterization and On-Line Prediction of Transient Thermal Field in Integrated Circuits Using Thermal System Identification. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2014 , 4, 37-45	1.7	2
39	A Wide Conversion Ratio, Extended Input 3.5- μ A Boost Regulator With 82% Efficiency for Low-Voltage Energy Harvesting. <i>IEEE Transactions on Power Electronics</i> , 2014 , 29, 4776-4786	7.2	20
38	A Variation-Aware Preferential Design Approach for Memory-Based Reconfigurable Computing. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2014 , 22, 2449-2461	2.6	1

37	Analysis of the Performance, Power, and Noise Characteristics of a CMOS Image Sensor With 3-D Integrated Image Compression Unit. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2014 , 4, 198-208	1.7	5
36	Guest Editorial Computing in Emerging Technologies (First Issue). <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , 2014 , 4, 377-379	5.2	
35	Ultra-low power electronics with Si/Ge tunnel FET 2014 ,		12
34	TSV-Aware Interconnect Distribution Models for Prediction of Delay and Power Consumption of 3-D Stacked ICs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2014 , 33, 1384-1395	2.5	21
33	Energy Introspector: A parallel, composable framework for integrated power-reliability-thermal modeling for multicore architectures 2014 ,		7
32	Application of Silicon-Germanium Source Tunnel-FET to Enable Ultralow Power Cellular Neural Network-Based Associative Memory. <i>IEEE Transactions on Electron Devices</i> , 2014 , 61, 3707-3715	2.9	27
31	Performance and Robustness of 3-D Integrated SRAM Considering Tier-to-Tier Thermal and Supply Crosstalk. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2013 , 3, 943-953	1.7	4
30	A 110nA synchronous boost regulator with autonomous bias gating for energy harvesting 2013 ,		2
29	Hotspot Cooling in Stacked Chips Using Thermoelectric Coolers. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2013 , 3, 759-767	1.7	23
28	Power Multiplexing for Thermal Field Management in Many-Core Processors. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2013 , 3, 94-104	1.7	3
27	Variation-Aware Clock Network Design Methodology for Ultralow Voltage (ULV) Circuits. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2012 , 31, 1222-1234	2.5	6
26	Thermal Investigation Into Power Multiplexing for Homogeneous Many-Core Processors. <i>Journal of Heat Transfer</i> , 2012 , 134,	1.8	7
25	Ultrathin Thermoelectric Devices for On-Chip Peltier Cooling. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2011 , 1, 1395-1405	1.7	49
24	Pre-Bond and Post-Bond Test and Signal Recovery Structure to Characterize and Repair TSV Defect Induced Signal Degradation in 3-D System. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2011 , 1, 1718-1727	1.7	42
23	A Scalable Design Methodology for Energy Minimization of STTRAM: A Circuit and Architecture Perspective. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2011 , 19, 809-817	2.6	27
22	Energy-Efficient Reconfigurable Computing Using a Circuit-Architecture-Software Co-Design Approach. <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , 2011 , 1, 369-380	5.2	16
21	Modeling and Analysis of Image Dependence and Its Implications for Energy Savings in Error Tolerant Image Processing. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2011 , 30, 1163-1172	2.5	9
20	Analysis and Design of Energy and Slew Aware Subthreshold Clock Systems. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2011 , 30, 1349-1358	2.5	8

19	Through-Oxide-Via-Induced Back-Gate Effect in 3-D Integrated FDSOI Devices. <i>IEEE Electron Device Letters</i> , 2011 , 32, 1020-1022	4.4	7
18	Fast and Accurate Analytical Modeling of Through-Silicon-Via Capacitive Coupling. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2011 , 1, 168-180	1.7	54
17	Design method and test structure to characterize and repair TSV defect induced signal degradation in 3D system 2010 ,		47
16	Postsilicon Adaptation for Low-Power SRAM under Process Variation. <i>IEEE Design and Test of Computers</i> , 2010 , 27, 26-35		2
15	Dual-Source-Line-Bias Scheme to Improve the Read Margin and Sensing Accuracy of STTRAM in Sub-90-nm Nodes. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2010 , 57, 208-212	3.5	3
14	Thermal mangament of multicore processors using power multiplexing 2010 ,		2
13	On-chip Peltier cooling using current pulse 2010 ,		6
12	Accuracy-aware SRAM: A reconfigurable low power SRAM architecture for mobile multimedia applications 2009 ,		18
11	A Generic Data-Driven Nonparametric Framework for Variability Analysis of Integrated Circuits in Nanometer Technologies. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2009 , 28, 1038-1046	2.5	6
10	Design of Sub-90 nm Low-Power and Variation Tolerant PD/SOI SRAM Cell Based on Dynamic Stability Metrics. <i>IEEE Journal of Solid-State Circuits</i> , 2009 , 44, 965-976	5.5	21
9	Device Design and Optimization Methodology for Leakage and Variability Reduction in Sub-45-nm FD/SOI SRAM. <i>IEEE Transactions on Electron Devices</i> , 2008 , 55, 152-162	2.9	7
8	Optimal Dual- V_{T} Design in Sub-100-nm PD/SOI and Double-Gate Technologies. <i>IEEE Transactions on Electron Devices</i> , 2008 , 55, 1161-1169	2.9	1
7	Reduction of Parametric Failures in Sub-100-nm SRAM Array Using Body Bias. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2008 , 27, 174-183	2.5	20
6	A generic method for variability analysis of nanoscale circuits 2008 ,		3
5	Profit Aware Circuit Design Under Process Variations Considering Speed Binning. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2008 , 16, 806-815	2.6	13
4	Design and Analysis of a Self-Repairing SRAM with On-Chip Monitor and Compensation Circuitry. <i>VLSI Test Symposium (VTS), Proceedings, IEEE</i> , 2008 ,		3
3	. <i>IEEE Transactions on Electron Devices</i> , 2007 , 54, 1409-1419	2.9	75
2	Design of a Process Variation Tolerant Self-Repairing SRAM for Yield Enhancement in Nanoscaled CMOS. <i>IEEE Journal of Solid-State Circuits</i> , 2007 , 42, 1370-1382	5.5	40

- 1 Impact of HKMG and FDSOI FeFET drain current variation in processing-in-memory architectures. *Journal of Materials Research*,1 2.5