Pavan Kumar Hanumolu

List of Publications by Year
in descending order

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54	2,046	201385	233125
papers	citations	27 h-index	45 g-index

54	54	54	1582
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 32-MHz, 34-Î¼W Temperature-Compensated RC Oscillator Using Pulse Density Modulated Resistors. IEEE Journal of Solid-State Circuits, 2022, 57, 1470-1479.	3.5	14
2	A 3.2-GHz 405 fs_{rms} Jitter â€“237.2 dB FoM_{JIT} Ring-Based Fractional-N Synthesizer. IEEE Journal of Solid-State Circuits, 2022, 57, 698-708.	3.5	5
3	A 5.2 Gb/s Receiver for Next-Generation 8K Displays in 180 nm CMOS Process. IEEE Journal of Solid-State Circuits, 2022, 57, 2521-2531.	3.5	2
4	A 16-Gb/s -11.6-dBm OMA Sensitivity 0.7-pJ/bit Optical Receiver in 65-nm CMOS Enabled by Duobinary Sampling. IEEE Journal of Solid-State Circuits, 2021, 56, 2795-2803.	3.5	7
5	A 91.15% Efficient 2.3â€“5-V Input 10â€“35-V Output Hybrid Boost Converter for LED-Driver Applications. IEEE Journal of Solid-State Circuits, 2021, 56, 3499-3510.	3.5	14
6	A 0.016 mm² 0.26-mu W/MHz 60â€“240-MHz Digital PLL With Delay-Modulating Clock Buffer in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 2186-2194.	3.5	2
7	A 2.5â€“5.75-GHz Ring-Based Injection-Locked Clock Multiplier With Background-Calibrated Reference Frequency Doubler. IEEE Journal of Solid-State Circuits, 2019, 54, 2049-2058.	3.5	34
8	Design of Crystal-Oscillator Frequency Quadrupler for Low-Jitter Clock Multipliers. IEEE Journal of Solid-State Circuits, 2019, 54, 65-74.	3.5	23
9	34-GBd Linear Transimpedance Amplifier for 200-Gb/s DP-16-QAM Optical Coherent Receivers. IEEE Journal of Solid-State Circuits, 2019, 54, 834-844.	3.5	37
10	A 10-Gb/s/ch, 0.6-pJ/bit/mm Power Scalable Rapid-ON/OFF Transceiver for On-Chip Energy Proportional Interconnects. IEEE Journal of Solid-State Circuits, 2018, 53, 873-883.	3.5	8
11	Low-Jitter Multi-Output All-Digital Clock Generator Using DTC-Based Open Loop Fractional Dividers. IEEE Journal of Solid-State Circuits, 2018, 53, 1806-1817.	3.5	35
12	A 0.45â€“0.7 V 1â€“6 Gb/s 0.29â€“0.58 pJ/b Source-Synchronous Transceiver Using Near-Threshold Operation. IEEE Journal of Solid-State Circuits, 2018, 53, 884-895.	3.5	12
13	A 10-MHz 2â€“800-mA 0.5â€“1.5-V 90% Peak Efficiency Time-Based Buck Converter With Seamless Transition Between PWM/PFM Modes. IEEE Journal of Solid-State Circuits, 2018, 53, 814-824.	3.5	51
14	Time-Based PWM Controller for Fully Integrated High Speed Switching DC-DC Converters â€” An Alternative to Conventional Analog and Digital Controllers. , 2018, , .		1
15	A 6.75â€“8.25-GHz â˜250-dB FoM Rapid ON/OFF Fractional-N Injection-Locked Clock Multiplier. IEEE Journal of Solid-State Circuits, 2018, 53, 1818-1829.	3.5	30
16	A 12-Gb/s -16.8-dBm OMA Sensitivity 23-mW Optical Receiver in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 445-457.	3.5	41
17	A 1.6ps peak-INL 5.3ns range two-step digital-to-time converter in 65nm CMOS. , 2018, , .		12
18	10.3 A 94.2%-peak-efficiency 1.53A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65nm CMOS. , 2017, , .		43

#	Article	IF	Citations
19	A 5GHz Digital Fractional- N PLL Using a 1-bit Deltaâ€“Sigma Frequency-to-Digital Converter in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2017, 52, 2306-2320.	3.5	7
20	A VCO Based Highly Digital Temperature Sensor With 0.034 Â°C/mV Supply Sensitivity. IEEE Journal of Solid-State Circuits, 2016, 51, 2651-2663.	3.5	81
21	A 2.0â€“5.5 GHz Wide Bandwidth Ring-Based Digital Fractional-N PLL With Extended Range Multi-Modulus Divider. IEEE Journal of Solid-State Circuits, 2016, 51, 1771-1784.	3.5	57
22	A 3.7 mW Low-Noise Wide-Bandwidth 4.5 GHz Digital Fractional-N PLL Using Time Amplifier-Based TDC. IEEE Journal of Solid-State Circuits, 2015, 50, 867-881.	3.5	212
23	A Burst-Mode Digital Receiver With Programmable Input Jitter Filtering for Energy Proportional Links. IEEE Journal of Solid-State Circuits, 2015, 50, 737-748.	3.5	22
24	A 7 Gb/s Embedded Clock Transceiver for Energy Proportional Links. IEEE Journal of Solid-State Circuits, 2015, 50, 3101-3119.	3.5	14
25	Design and Analysis of Low-Power High-Frequency Robust Sub-Harmonic Injection-Locked Clock Multipliers. IEEE Journal of Solid-State Circuits, 2015, 50, 3160-3174.	3.5	51
26	A 5 Gb/s, 10 ns Power-On-Time, 36 <formula formulatype="inline"> <tex Notation="TeX">mu</tex></formula>W Off-State Power, Fast Power-On Transmitter for Energy Proportional Links. IEEE Journal of Solid-State Circuits, 2014, 49, 2243-2258.	3.5	7
27	A Reference-Less Clock and Data Recovery Circuit Using Phase-Rotating Phase-Locked Loop. IEEE Journal of Solid-State Circuits, 2014, 49, 1036-1047.	3.5	41
28	A Noise-Shaping Time-to-Digital Converter Using Switched-Ring Oscillatorsâ€”Analysis, Design, and Measurement Techniques. IEEE Journal of Solid-State Circuits, 2014, 49, 1184-1197.	3.5	66
29	Clock Multiplication Techniques Using Digital Multiplying Delay-Locked Loops. IEEE Journal of Solid-State Circuits, 2013, 48, 1416-1428.	3.5	75
30	A 12.5-bit 4 MHz 13.8 mW MASH $Delta Sigma$ Modulator With Multirated VCO-Based ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1604-1613.	3.5	24
31	A 16-mW 78-dB SNDR 10-MHz BW CT $Delta Sigma$ ADC Using Residue-Cancelling VCO-Based Quantizer. IEEE Journal of Solid-State Circuits, 2012, 47, 2916-2927.	3.5	99
32	Analog Filter Design Using Ring Oscillator Integrators. IEEE Journal of Solid-State Circuits, 2012, 47, 3120-3129.	3.5	76
33	Rail-to-Rail Input Pipelined ADC Incorporating Multistage Signal Mapping. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 558-562.	2.2	2
34	A 1.2-A Buck-Boost LED Driver With On-Chip Error Averaged SenseFET-Based Current Sensing Technique. IEEE Journal of Solid-State Circuits, 2011, 46, 2772-2783.	3.5	39
35	Introduction to the Special Issue on the 2010 IEEE Custom Integrated Circuits Conference. IEEE Journal of Solid-State Circuits, 2011, 46, 1770-1771.	3.5	0
36	A 0.4-to-3 GHz Digital PLL With PVT Insensitive Supply Noise Cancellation Using Deterministic Background Calibration. IEEE Journal of Solid-State Circuits, 2011, 46, 2759-2771.	3.5	45

#	Article	IF	Citations
37	A 0.5-to-2.5 Gb/s Reference-Less Half-Rate Digital CDR With Unlimited Frequency Acquisition Range and Improved Input Duty-Cycle Error Tolerance. IEEE Journal of Solid-State Circuits, 2011, 46, 3150-3162.	3.5	64
38	Continuous-Time Input Pipeline ADCs. IEEE Journal of Solid-State Circuits, 2010, 45, 1456-1468.	3.5	27
39	Introduction to the Special Issue on the IEEE 2009 Custom Integrated Circuits Conference. IEEE Journal of Solid-State Circuits, 2010, 45, 1425-1426.	3.5	0
40	A Low Power Pipelined ADC Using Capacitor and Opamp Sharing Technique With a Scheme to Cancel the Effect of Signal Dependent Kickback. IEEE Journal of Solid-State Circuits, 2009, 44, 2392-2401.	3.5	32
41	Method for a Constant Loop Bandwidth in LC-VCO PLL Frequency Synthesizers. IEEE Journal of Solid-State Circuits, 2009, 44, 427-435.	3.5	82
42	A Digital PLL With a Stochastic Time-to-Digital Converter. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1612-1621.	3.5	86
43	Automated Design and Optimization of Low-Noise Oscillators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 609-622.	1.9	5
44	Low-Power Supply-Regulation Techniques for Ring Oscillators in Phase-Locked Loops Using a Split-Tuned Architecture. IEEE Journal of Solid-State Circuits, 2009, 44, 2169-2181.	3.5	59
45	A 10 MS/s 11-bit 0.19 mm^{2} Algorithmic ADC With Improved Clocking Scheme. IEEE Journal of Solid-State Circuits, 2009, 44, 2348-2355.	3.5	23
46	An 8$,imes,$5 Gb/s Parallel Receiver With Collaborative Timing Recovery. IEEE Journal of Solid-State Circuits, 2009, 44, 3120-3130.	3.5	23
47	Noise tolerant oscillator design using perturbation projection vector analysis. , 2008, , .		0
48	Sensitivity Analysis for Oscillators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1521-1534.	1.9	13
49	A Wide-Tracking Range Clock and Data Recovery Circuit. IEEE Journal of Solid-State Circuits, 2008, 43, 425-439.	3.5	89
50	A 0.9 V 92 dB Double-Sampled Switched-RC Delta-Sigma Audio ADC. IEEE Journal of Solid-State Circuits, 2008, 43, 1195-1206.	3.5	56
51	A Design Procedure for All-Digital Phase-Locked Loops Based on a Charge-Pump Phase-Locked-Loop Analogy. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 247-251.	2.3	116
52	A 0.5-GHz to 2.5-GHz PLL With Fully Differential Supply Regulated Tuning. IEEE Journal of Solid-State Circuits, 2006, 41, 2720-2728.	3.5	53
53	EQUALIZERS FOR HIGH-SPEED SERIAL LINKS. Selected Topics in Electornics and Systems, 2006, , 175-204.	0.2	0
54	EQUALIZERS FOR HIGH-SPEED SERIAL LINKS. International Journal of High Speed Electronics and Systems, 2005, 15, 429-458.	0.3	29