Dong-Jin Chang

List of Publications by Year
in descending order

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10 papers	175 citations	1478505 6 h-index	1588992 8 g-index
10 all docs	10 docs citations	10 times ranked	200 citing authors

#	Article	IF	Citations
1	MixedNet: Network Design Strategies for Cost-Effective Quantized CNNs. IEEE Access, 2021, 9, 117554-117564.	4.2	0
2	A 28-nm 10-b 2.2-GS/s 18.2-mW Relative-Prime Time-Interleaved Sub-Ranging SAR ADC With On-Chip Background Skew Calibration. IEEE Journal of Solid-State Circuits, 2021, 56, 2691-2700.	5.4	10
3	Compact Mixed-Signal Convolutional Neural Network Using a Single Modular Neuron. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 5189-5199.	5.4	1
4	A 40-nm CMOS 12b 120-MS/s Nonbinary SAR-Assisted SAR ADC With Double Clock-Rate Coarse Decision. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2833-2837.	3.0	15
5	A 65-nm CMOS 6-bit 2.5-GS/s 7.5-mW 8<inline-formula> <tex-math notation="LaTeX">$imes$ </tex-math> </inline-formula> Time-Domain Interpolating Flash ADC With Sequential Slope-Matching Offset Calibration. IEEE Journal of Solid-State Circuits, 2019, 54, 288-297.	5.4	27
6	A Single-Supply Buffer-Embedding SAR ADC with Skip-Reset having Inherent Chopping Capability. , 2019, , .		5
7	A Reusable Code-Based SAR ADC Design With CDAC Compiler and Synthesizable Analog Building Blocks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1904-1908.	3.0	29
8	A 65 nm 0.08-to-680 MHz Low-Power Synthesizable MDLL With Nested-Delay Cell and Background Static Phase Offset Calibration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 281-285.	3.0	6
9	Normalized-Full-Scale-Referencing Digital-Domain Linearity Calibration for SAR ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 322-332.	5.4	17
10	A 0.6 V 12 b 10 MS/s Low-Noise Asynchronous SAR-Assisted Time-Interleaved SAR (SATI-SAR) ADC. IEEE Journal of Solid-State Circuits, 2016, 51, 1826-1839.	5.4	65