## Vivienne Sze

List of Publications by Year in descending order

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VIVIENNE SZE

#	Article	IF	CITATIONS
1	Efficient Processing of Deep Neural Networks: A Tutorial and Survey. Proceedings of the IEEE, 2017, 105, 2295-2329.	21.3	2,217
2	Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks. IEEE Journal of Solid-State Circuits, 2017, 52, 127-138.	5.4	1,877
3	Eyeriss. Computer Architecture News, 2016, 44, 367-379.	2.5	833
4	Eyeriss v2: A Flexible Accelerator for Emerging Deep Neural Networks on Mobile Devices. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 292-308.	3.6	609
5	Designing Energy-Efficient Convolutional Neural Networks Using Energy-Aware Pruning. , 2017, , .		374
6	High Throughput CABAC Entropy Coding in HEVC. IEEE Transactions on Circuits and Systems for Video Technology, 2012, 22, 1778-1791.	8.3	160
7	Navion: A 2-mW Fully Integrated Real-Time Visual-Inertial Odometry Accelerator for Autonomous Navigation of Nano Drones. IEEE Journal of Solid-State Circuits, 2019, 54, 1106-1119.	5.4	72
8	Efficient Processing of Deep Neural Networks. Synthesis Lectures on Computer Architecture, 2020, 15, 1-341.	1.3	72
9	Low-Power Impulse UWB Architectures and Circuits. Proceedings of the IEEE, 2009, 97, 332-352.	21.3	70
10	A 249-Mpixel/s HEVC Video-Decoder Chip for 4K Ultra-HD Applications. IEEE Journal of Solid-State Circuits, 2014, 49, 61-72.	5.4	59
11	A 0.7-V 1.8-mW H.264/AVC 720p Video Decoder. IEEE Journal of Solid-State Circuits, 2009, 44, 2943-2956.	5.4	44
12	Designing Hardware for Machine Learning: The Important Role Played by Circuit Designers. IEEE Solid-State Circuits Magazine, 2017, 9, 46-54.	0.4	42
13	How to Evaluate Deep Neural Network Processors: TOPS/W (Alone) Considered Harmful. IEEE Solid-State Circuits Magazine, 2020, 12, 28-41.	0.4	40
14	An Energy-Efficient Hardware Implementation of HOG-Based Object Detection at 1080HD 60 fps with Multi-Scale Support. Journal of Signal Processing Systems, 2016, 84, 325-337.	2.1	39
15	Towards closing the energy gap between HOG and CNN features for embedded vision. , 2017, , .		35
16	A Deeply Pipelined CABAC Decoder for HEVC Supporting Level 6.2 High-Tier Applications. IEEE Transactions on Circuits and Systems for Video Technology, 2015, 25, 856-868.	8.3	34
17	Freely scalable and reconfigurable optical hardware for deep learning. Scientific Reports, 2021, 11, 3144.	3.3	32
18	Measuring Saccade Latency Using Smartphone Cameras. IEEE Journal of Biomedical and Health Informatics, 2020, 24, 885-897.	6.3	20

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19	FSMI: Fast computation of Shannon mutual information for information-theoretic mapping. International Journal of Robotics Research, 2020, 39, 1155-1177.	8.5	19
20	Energy and area-efficient hardware implementation of HEVC inverse transform and dequantization. , 2014, , .		16
21	Rotate intra block copy for still image coding. , 2015, , .		15
22	Sparseloop: An Analytical, Energy-Focused Design Space Exploration Methodology for Sparse Tensor Accelerators. , 2021, , .		11
23	Low Power Depth Estimation of Rigid Objects for Time-of-Flight Imaging. IEEE Transactions on Circuits and Systems for Video Technology, 2020, 30, 1524-1534.	8.3	9
24	Low power depth estimation for time-of-flight imaging. , 2017, , .		6
25	A fully-integrated energy-efficient H.265/HEVC decoder with eDRAM for wearable devices. , 2017, , .		6
26	Enabling Saccade Latency Measurements with Consumer-Grade Cameras. , 2018, , .		4
27	Depth Estimation of Non-Rigid Objects for Time-Of-Flight Imaging. , 2018, , .		4
28	A Fully Integrated Energy-Efficient H.265/HEVC Decoder With eDRAM for Wearable Devices. IEEE Journal of Solid-State Circuits, 2018, 53, 2368-2377.	5.4	4
29	App-Based Saccade Latency and Directional Error Determination Across the Adult Age Spectrum. IEEE Transactions on Biomedical Engineering, 2022, 69, 1029-1039.	4.2	4
30	Architecture-Level Energy Estimation for Heterogeneous Computing Systems. , 2021, , .		2