

# Andrés Otero

## List of Publications by Year in descending order

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Version: 2024-02-01

40  
papers

444  
citations

1464605

7  
h-index

1051228

16  
g-index

41  
all docs

41  
docs citations

41  
times ranked

349  
citing authors

#	ARTICLE	IF	CITATIONS
1	Exploiting Hardware-Based Data-Parallel and Multithreading Models for Smart Edge Computing in Reconfigurable FPGAs. IEEE Transactions on Computers, 2022, 71, 2903-2914.	2.4	1
2	A Machine-Learning-Based Distributed System for Fault Diagnosis With Scalable Detection Quality in Industrial IoT. IEEE Internet of Things Journal, 2021, 8, 4339-4352.	5.5	28
3	A Machine Learning-based Methodology for in-Process Fluid Characterisation with Photonic Sensors. IEEE Sensors Journal, 2021, , 1-1.	2.4	0
4	Multi-grain reconfigurable and scalable overlays for hardware accelerator composition. Journal of Systems Architecture, 2021, 121, 102302.	2.5	2
5	Run-Time Monitoring and ML-Based Modeling in Reconfigurable Multi-Accelerator Systems. , 2021, , .		0
6	Exploiting Multi-Level Parallelism for Run-Time Adaptive Inverse Kinematics on Heterogeneous MPSoCs. IEEE Access, 2020, 8, 118707-118724.	2.6	6
7	An Integrated Approach and Tool Support for the Design of FPGA-Based Multi-Grain Reconfigurable Systems. IEEE Access, 2020, 8, 202133-202152.	2.6	3
8	Lossy Hyperspectral Image Compression on a Reconfigurable and Fault-Tolerant FPGA-Based Adaptive Computing Platform. Electronics (Switzerland), 2020, 9, 1576.	1.8	7
9	A Dynamically Reconfigurable BbNN Architecture for Scalable Neuroevolution in Hardware. Electronics (Switzerland), 2020, 9, 803.	1.8	4
10	Run-Time Reconfigurable MPSoC-Based On-Board Processor for Vision-Based Space Navigation. IEEE Access, 2020, 8, 59891-59905.	2.6	19
11	Automated Toolchain for Enhanced Productivity in Reconfigurable Multi-accelerator Systems. Lecture Notes in Computer Science, 2020, , 45-60.	1.0	0
12	Automated Tool and Runtime Support for Fine-Grain Reconfiguration in Highly Flexible Reconfigurable Systems. , 2019, , .		2
13	IMPRESS: Automated Tool for the Implementation of Highly Flexible Partial Reconfigurable Systems with Xilinx Vivado. , 2018, , .		14
14	Performance Analysis of SEE Mitigation Techniques on Zynq Ultrascale + Hardened Processing Fabrics. , 2018, , .		1
15	A Runtime-Scalable and Hardware-Accelerated Approach to On-Board Linear Unmixing of Hyperspectral Images. Remote Sensing, 2018, 10, 1790.	1.8	3
16	FPGA-Based High-Performance Embedded Systems for Adaptive Edge Computing in Cyber-Physical Systems: The ARTICO3 Framework. Sensors, 2018, 18, 1877.	2.1	56
17	Dynamic reconfiguration under RTEMS for fault mitigation and functional adaptation in SRAM-based SoPCs for space systems. , 2017, , .		7
18	A scalable H.264/AVC deblocking filter architecture. Journal of Real-Time Image Processing, 2016, 12, 81-105.	2.2	2

#	ARTICLE	IF	CITATIONS
19	Sophisticated security verification on routing repaired balanced cell-based dual-rail logic against side channel analysis. IET Information Security, 2015, 9, 1-13.	1.1	3
20	Fast and compact evolvable systolic arrays on dynamically reconfigurable FPGAs. , 2015, , .		5
21	A dynamically adaptable bus architecture for trading-off among performance, consumption and dependability in Cyber-Physical Systems. , 2014, , .		6
22	Customized and automated routing repair toolset towards side-channel analysis resistant dual rail logic. Microprocessors and Microsystems, 2014, 38, 899-910.	1.8	7
23	Self-Reconfigurable Evolvable Hardware System for Adaptive Image Processing. IEEE Transactions on Computers, 2013, 62, 1481-1493.	2.4	40
24	A Novel FPGA-based Evolvable Hardware System Based on Multiple Processing Arrays. , 2013, , .		5
25	A scalable evolvable hardware processing array. , 2013, , .		5
26	A self-adaptive image processing application based on evolvable and scalable hardware. , 2013, , .		2
27	Architectural evaluation of dynamic and partial reconfigurable systems designed with DREAMS tool. , 2013, , .		0
28	Implementation techniques for evolvable HW systems: virtual VS. dynamic reconfiguration. , 2012, , .		8
29	On the automatic integration of hardware accelerators into FPGA-based embedded systems. , 2012, , .		10
30	Dreams: A tool for the design of dynamically reconfigurable embedded and modular systems. , 2012, , .		18
31	Using SRAM Based FPGAs for Power-Aware High Performance Wireless Sensor Networks. Sensors, 2012, 12, 2667-2692.	2.1	43
32	Automatic generation of identical routing pairs for FPGA implemented DPL logic. , 2012, , .		19
33	Evolvable 2D computing matrix model for intrinsic evolution in commercial FPGAs with native reconfiguration support. , 2011, , .		11
34	Cost and energy efficient reconfigurable embedded platform using Spartan-6 FPGAs. , 2011, , .		4
35	Fault Tolerance Analysis and Self-Healing Strategy of Autonomous, Evolvable Hardware Systems. , 2011, , .		28
36	A fast Reconfigurable 2D HW core architecture on FPGAs for evolvable Self-Adaptive Systems. , 2011, , .		14

#	ARTICLE	IF	CITATIONS
37	Adaptable Security in Wireless Sensor Networks by Using Reconfigurable ECC Hardware Coprocessors. International Journal of Distributed Sensor Networks, 2010, 6, 740823.	1.3	30
38	A Modular Peripheral to Support Self-Reconfiguration in SoCs. , 2010, , .		18
39	Run-Time Scalable Systolic Coprocessors for Flexible Multimedia SoPCs. , 2010, , .		8
40	Generic Systolic Array for Run-Time Scalable Cores. Lecture Notes in Computer Science, 2010, , 4-16.	1.0	4