Jian F Zhang

List of Publications by Year
in descending order

149 papers	2,215 citations	201658 27 h-index	330122 37 g-index
150 all docs	150 docs citations	150 times ranked	1178 citing authors

#	Article	IF	Citations
1	A Probability-Based Strong Physical Unclonable Function With Strong Machine Learning Immunity. IEEE Electron Device Letters, 2022, 43, 138-141.	3.9	0
2	Bias Temperature Instability of MOSFETs: Physical Processes, Models, and Prediction. Electronics (Switzerland), 2022, 11, 1420.	3.1	6
3	Impact of Relaxation on the Performance of GeSe True Random Number Generator Based on Ovonic Threshold Switching. IEEE Electron Device Letters, 2022, 43, 1061-1064.	3.9	5
4	An Integral Methodology for Predicting Long-Term RTN. IEEE Transactions on Electron Devices, 2022, 69, 3869-3875.	3.0	3
5	Realization of NOR logic using Cu/ZnO/Pt CBRAM. , 2022, , .		0
6	Realization of Logical NOT Based on Standard DRAM Cells for security-centric Compute-in-Memory applications. , 2022, , .		0
7	On the Accuracy in Modeling the Statistical Distribution of Random Telegraph Noise Amplitude. IEEE Access, 2021, 9, 43551-43561.	4.2	9
8	A Comparative Study of AC Positive Bias Temperature Instability of Germanium nMOSFETs With GeOâ„/Ge and Si-cap/Ge Gate Stack. IEEE Journal of the Electron Devices Society, 2021, 9, 539-544.	2.1	0
9	Cycling Induced Metastable Degradation in GeSe Ovonic Threshold Switching Selector. IEEE Electron Device Letters, 2021, 42, 1448-1451.	3.9	10
10	Understanding Generated RTN as an Entropy Source for True Random Number Generators. , 2021, , .		1
11	An integrated method for extracting the statistical distribution of RTN time constants. , 2021, , .		0
12	Investigation on the Implementation of Stateful Minority Logic for Future In-Memory Computing. IEEE Access, 2021, 9, 168648-168655.	4.2	0
13	GeSe-Based Ovonic Threshold Switching Volatile True Random Number Generator. IEEE Electron Device Letters, 2020, 41, 228-231.	3.9	17
14	Random-telegraph-noise-enabled true random number generator for hardware security. Scientific Reports, 2020, 10, 17210.	3.3	12
15	Exploring the Impact of Random Telegraph Noise-Induced Accuracy Loss on Resistive RAM-Based Deep Neural Network. IEEE Transactions on Electron Devices, 2020, 67, 3335-3340.	3.0	15
16	Stochastic Computing Based on Volatile GeSe Ovonic Threshold Switching Selectors. IEEE Electron Device Letters, 2020, 41, 1496-1499.	3.9	3
17	An Assessment of the Statistical Distribution of Random Telegraph Noise Time Constants. IEEE Access, 2020, 8, 182273-182282.	4.2	12
18	A Fast Extraction Method of Energy Distribution of Border Traps in AlGaN/GaN MIS-HEMT. IEEE Journal of the Electron Devices Society, 2020, 8, 905-910.	2.1	5

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19	True Random Number Generator (TRNG) for Secure Communications in the Era of IoT. , 2020, , .		4
20	Defect loss and its physical processes. , 2020, , .		0
21	Dependence of Switching Probability on Operation Conditions in Ge_xSe_{1â€“x}Ovonic Threshold Switching Selectors. IEEE Electron Device Letters, 2019, 40, 1269-1272.	3.9	23
22	RTN in GexSe1-x OTS selector devices. Microelectronic Engineering, 2019, 215, 110990.	2.4	3
23	A Dual-Point Technique for the Entire I_Dâ€“V_G Characterization Into Subthreshold Region Under Random Telegraph Noise Condition. IEEE Electron Device Letters, 2019, 40, 674-677.	3.9	9
24	Trigger-When-Charged: A Technique for Directly Measuring RTN and BTI-Induced Threshold Voltage Fluctuation Under Use-<inline-formula> <tex-math notation="LaTeX">${V}_{dd}$ </tex-math> </inline-formula>. IEEE Transactions on Electron Devices, 2019, 66, 1482-1488.	3.0	12
25	An assessment of RTN-induced threshold voltage jitter. , 2019, , .		0
26	Understanding lifetime prediction methodology for In0.53Ga0.47As nFETs under Positive Bias Temperature Instability (PBTI) condition. , 2019, , .		0
27	TDDB Mechanism in a-Si/TiO₂ Nonfilamentary RRAM Device. IEEE Transactions on Electron Devices, 2019, 66, 777-784.	3.0	10
28	The Over-Reset Phenomenon in Ta₂O₅ RRAM Device Investigated by the RTN-Based Defect Probing Technique. IEEE Electron Device Letters, 2018, 39, 955-958.	3.9	18
29	Investigation of Preexisting and Generated Defects in Nonfilamentary a-Si/TiO₂ RRAM and Their Impacts on RTN Amplitude Distribution. IEEE Transactions on Electron Devices, 2018, 65, 970-977.	3.0	13
30	As-grown-generation (AG) model of NBTI: A shift from fitting test data to prediction. Microelectronics Reliability, 2018, 80, 109-123.	1.7	25
31	A low-power and high-speed True Random Number Generator using generated RTN. , 2018, , .		22
32	A framework for defects in PBTI and hot carrier ageing. , 2018, , .		0
33	Impact of RTN on Pattern Recognition Accuracy of RRAM-Based Synaptic Neural Network. IEEE Electron Device Letters, 2018, 39, 1652-1655.	3.9	38
34	Predictive As-grown-generation model for NBTI of advanced CMOS devices and circuits. , 2018, , .		0
35	As-grown-Generation Model for Positive Bias Temperature Instability. IEEE Transactions on Electron Devices, 2018, 65, 3662-3668.	3.0	22
36	Key Issues and Solutions for Characterizing Hot Carrier Aging of Nanometer Scale nMOSFETs. IEEE Transactions on Electron Devices, 2017, 64, 2478-2484.	3.0	22

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37	Reliable Time Exponents for Long Term Prediction of Negative Bias Temperature Instability by Extrapolation. IEEE Transactions on Electron Devices, 2017, 64, 1467-1473.	3.0	35
38	NBTI-Generated Defects in Nanoscaled Devices: Fast Characterization Methodology and Modeling. IEEE Transactions on Electron Devices, 2017, 64, 4011-4017.	3.0	23
39	Hot carrier aging of nano-scale devices: Characterization method, statistical variation, and their impact on use voltage. , 2017, , .		0
40	Time-dependent variability in RRAM-based analog neuromorphic system for pattern recognition. , 2017, , .		29
41	Probing the Critical Region of Conductive Filament in Nanoscale HfO₂ Resistive-Switching Device by Random Telegraph Signals. IEEE Transactions on Electron Devices, 2017, 64, 4099-4105.	3.0	11
42	A Comparative Study of Defect Energy Distribution and Its Impact on Degradation Kinetics in GeO2/Ge and SiON/Si pMOSFETs. IEEE Transactions on Electron Devices, 2016, 63, 3830-3836.	3.0	9
43	Insight Into Electron Traps and Their Energy Distribution Under Positive Bias Temperature Stress and Hot Carrier Aging. IEEE Transactions on Electron Devices, 2016, 63, 3642-3648.	3.0	28
44	Understanding charge traps for optimizing Si-passivated Ge nMOSFETs. , 2016, , .		15
45	RTN-based defect tracking technique: Experimentally probing the spatial and energy profile of the critical filament region and its correlation with HfO<inf>2</inf>RRAM switching operation and failure mechanism. , 2016, , .		20
46	Hot carrier aging of nano-meter devices. , 2016, , .		0
47	Impact of Hot Carrier Aging on Random Telegraph Noise and Within a Device Fluctuation. IEEE Journal of the Electron Devices Society, 2016, 4, 15-21.	2.1	8
48	NBTI prediction and its induced time dependent variation. , 2015, , .		0
49	A test-proven As-grown-Generation (A-G) model for predicting NBTI under use-bias. , 2015, , .		14
50	AC NBTI of Ge pMOSFETs: Impact of energy alternating defects on lifetime prediction. , 2015, , .		4
51	An Investigation on Border Traps in IIIâ€“V MOSFETs With an In_{0.53}Ga_{0.47}As Channel. IEEE Transactions on Electron Devices, 2015, 62, 3633-3639.	3.0	44
52	A Discharge-Based Pulse Technique for Probing the Energy Distribution of Positive Charges in Gate Dielectric. IEEE Transactions on Semiconductor Manufacturing, 2015, 28, 221-226.	1.7	5
53	ESD characterization of planar InGaAs devices. , 2015, , .		1
54	Development of a Technique for Characterizing Bias Temperature Instability-Induced Device-to-Device Variation at SRAM-Relevant Conditions. IEEE Transactions on Electron Devices, 2014, 61, 3081-3089.	3.0	24

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55	Characterization of Negative-Bias Temperature Instability of Ge MOSFETs With <inline-formula> <tex-math notation="TeX">${m GeO}_{2}/{m Al}_{2}{m O}_{3}$ </tex-math></inline-formula> Stack. IEEE Transactions on Electron Devices, 2014, 61, 1307-1315.	3.0	9
56	NBTI of Ge pMOSFETs: Understanding defects and enabling lifetime prediction. , 2014, , .		4
57	Time-dependent variation: A new defect-based prediction methodology. , 2014, , .		13
58	New insights into the design for end-of-life variability of NBTI in scaled high-κ/metal-gate Technology for the nano-reliability era. , 2014, , .		8
59	Energy Distribution of Positive Charges in <formula formulatype="inline"> <tex Notation="TeX">${m Al}_{2}{m O}_{3}{m GeO}_{2}/{m Ge}$</tex></formula> pMOSFETs. IEEE Electron Device Letters, 2014, 35, 160-162.	3.9	16
60	Evaluation and Solutions for P/E Window Instability Induced by Electron Trapping in High-<inline-formula> <tex-math notation="TeX">$kappa$ </tex-math></inline-formula> Intergate Dielectrics of Flash Memory Cells. IEEE Transactions on Electron Devices, 2014, 61, 1299-1306.	3.0	2
61	Experimental Evidence Toward Understanding Charge Pumping Signals in 3-D Devices With Poly-Si Channel. IEEE Transactions on Electron Devices, 2014, 61, 1501-1507.	3.0	4
62	Energy distribution of positive charges in high-k dielectric. Microelectronics Reliability, 2014, 54, 2329-2333.	1.7	4
63	Optimization of inter-gate-dielectrics in hybrid float gate devices to reduce window instability during memory operations. Microelectronics Reliability, 2014, 54, 2258-2261.	1.7	1
64	Time-dependent device-to-device variation accounting for within-device fluctuation (TVF): A new characterization technique. , 2014, , .		0
65	Oxide Defects. , 2014, , 253-285.		3
66	Observation of the Ambient Effect in BTI Characteristics of Back-Gated Single Layer Graphene Field Effect Transistors. IEEE Transactions on Electron Devices, 2013, 60, 2682-2686.	3.0	14
67	Statistical characterization of vertical poly-Si channel using charge pumping technique for 3D flash memory optimization. Microelectronic Engineering, 2013, 109, 39-42.	2.4	11
68	New Insights Into Defect Loss, Slowdown, and Device Lifetime Enhancement. IEEE Transactions on Electron Devices, 2013, 60, 413-419.	3.0	17
69	Energy Distribution of Positive Charges in Gate Dielectric: Probing Technique and Impacts of Different Defects. IEEE Transactions on Electron Devices, 2013, 60, 1745-1753.	3.0	50
70	Towards understanding hole traps and NBTI of Ge/GeO2/Al2O3 structure. Microelectronic Engineering, 2013, 109, 43-45.	2.4	1
71	Read and Pass Disturbance in the Programmed States of Floating Gate Flash Memory Cells With High-<formula formulatype="inline"><tex Notation="TeX">$kappa$</tex></formula> Interpoly Gate Dielectric Stacks. IEEE Transactions on Electron Devices, 2013, 60, 2261-2267.	3.0	7
72	Defect Losses under Different Processes, Stress, Recovery, and Anneal Conditions. ECS Transactions, 2013, 52, 929-934.	0.5	0

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73	New Analysis Method for Time-Dependent Device-To-Device Variation Accounting for Within-Device Fluctuation. IEEE Transactions on Electron Devices, 2013, 60, 2505-2511.	3.0	34
74	Characterization of Electron Traps in Si-Capped Ge MOSFETs With $hbox{HfO}_{2}/hbox{SiO}_{2}$ Gate Stack. IEEE Electron Device Letters, 2012, 33, 1681-1683.	3.9	14
75	$V_{m th}$ Shift in Single-Layer Graphene Field-Effect Transistors and Its Correlation With Raman Inspection. IEEE Transactions on Device and Materials Reliability, 2012, 12, 478-481.	2.0	13
76	Positive Bias-Induced $V_{m th}$ Instability in Graphene Field Effect Transistors. IEEE Electron Device Letters, 2012, 33, 339-341.	3.9	15
77	Defect Loss: A New Concept for Reliability of MOSFETs. IEEE Electron Device Letters, 2012, 33, 480-482.	3.9	28
78	Interface States Beyond Band Gap and Their Impact on Charge Carrier Mobility in MOSFETs. IEEE Transactions on Electron Devices, 2012, 59, 783-790.	3.0	7
79	Investigation of Abnormal $V_{m TH}/V_{m FB}$ Shifts Under Operating Conditions in Flash Memory Cells With $ hbox{Al}_{2}hbox{O}_{3}$ High-$kappa$ Gate Stacks. IEEE Transactions on Electron Devices, 2012, 59, 1870-1877.	3.0	10
80	A New Mobility Extraction Technique Based on Simultaneous Ultrafast I_{d}â€“V_{g} and $C_{m cg}$â€“V_{g} Measurements in MOSFETs. IEEE Transactions on Electron Devices, 2012, 59, 1906-1914.	3.0	12
81	Abnormal V<inf>TH</inf>/V<inf>FB</inf> shift caused by as-grown mobile charges in Al<inf>2</inf>O<inf>3</inf> and its impacts on Flash memory cell operations. , 2011, , .		1
82	Electron Trapping in HfAlO High-$kappa$ Stack for Flash Memory Applications: An Origin of $V_{m th}$ Window Closure During Cycling Operations. IEEE Transactions on Electron Devices, 2011, 58, 1344-1351.	3.0	14
83	A Single Pulse Charge Pumping Technique for Fast Measurements of Interface States. IEEE Transactions on Electron Devices, 2011, 58, 1490-1498.	3.0	48
84	Development of a Fast Technique for Characterizing Interface States. ECS Transactions, 2011, 35, 81-93.	0.5	1
85	Energy and Spatial Distributions of Electron Traps Throughout $hbox{SiO}_{2}/hbox{Al}_{2}hbox{O}_{3}$ Stacks as the IPD in Flash Memory Application. IEEE Transactions on Electron Devices, 2010, 57, 288-296.	3.0	33
86	NBTI Lifetime Prediction and Kinetics at Operation Bias Based on Ultrafast Pulse Measurement. IEEE Transactions on Electron Devices, 2010, 57, 228-237.	3.0	55
87	A New Multipulse Technique for Probing Electron Trap Energy Distribution in High- $kappa$ Materials for Flash Memory Application. IEEE Transactions on Electron Devices, 2010, 57, 2484-2492.	3.0	23
88	NBTI degradation effect on advanced-process 45nm high-k PMOSFETs with geometric and process variations. Microelectronics Reliability, 2010, 50, 1283-1289.	1.7	23
89	An assessment of the mobility degradation induced by remote charge scattering. Applied Physics Letters, 2009, 95, 263502.	3.3	9
90	On the activation and passivation of precursors for process-induced positive charges in Hf-dielectric stacks. Journal of Applied Physics, 2009, 105, 054505.	2.5	3

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91	An Analysis of the NBTI-Induced Threshold Voltage Shift Evaluated by Different Techniques. IEEE Transactions on Electron Devices, 2009, 56, 1086-1093.	3.0	42
92	Defects and instabilities in Hf-dielectric/SiON stacks (Invited Paper). Microelectronic Engineering, 2009, 86, 1883-1887.	2.4	39
93	Impact of PDA temperature on electron trap energy and spatial distributions in SiO2/Al2O3 stack as the IPD in Flash memory cells. Microelectronic Engineering, 2009, 86, 1834-1837.	2.4	3
94	A discharge-based multi-pulse technique (DMP) for probing electron trap energy distribution in high-k materials for Flash memory application. , 2009, , .		8
95	Reliability degradation of thin HfO2/SiO2 gate stacks by remote RF hydrogen and deuterium plasma treatment. Thin Solid Films, 2008, 517, 207-208.	1.8	10
96	Stress-Induced Positive Charge in Hf-Based Gate Dielectrics: Impact on Device Performance and a Framework for the Defect. IEEE Transactions on Electron Devices, 2008, 55, 1647-1656.	3.0	44
97	Dominant Layer for Stress-Induced Positive Charges in Hf-Based Gate Stacks. IEEE Electron Device Letters, 2008, 29, 1360-1363.	3.9	34
98	Two-Pulse Câ€“V : A New Method for Characterizing Electron Traps in the Bulk of $ hbox{SiO}_{2}/hbox{high-}kappa$ Dielectric Stacks. IEEE Electron Device Letters, 2008, 29, 1043-1046.	3.9	55
99	Impact of different defects on the kinetics of negative bias temperature instability of hafnium stacks. Applied Physics Letters, 2008, 92, 013501.	3.3	9
100	Process-induced positive charges in Hf-based gate stacks. Journal of Applied Physics, 2008, 103, 014507.	2.5	8
101	On positive charge formed under negative bias temperature stress. Journal of Applied Physics, 2007, 101, 024516.	2.5	28
102	Threshold voltage instability of p-channel metal-oxide-semiconductor field effect transistors with hafnium based dielectrics. Applied Physics Letters, 2007, 90, 143502.	3.3	13
103	Effects of Measurement Temperature on NBTI. IEEE Electron Device Letters, 2007, 28, 298-300.	3.9	36
104	Impact of process conditions on interface and high-Î¹ trap density studied by variable Tcharge-Tdischarge charge pumping (VT2CP). Microelectronic Engineering, 2007, 84, 1951-1955.	2.4	12
105	Hydrogen induced positive charge in Hf-based dielectrics. Microelectronic Engineering, 2007, 84, 2354-2357.	2.4	5
106	Reliability nano-characterization of thin SiO2 and HfSixOy/SiO2 gate stacks. Microelectronic Engineering, 2007, 84, 2290-2293.	2.4	13
107	Real-time observation of charging dynamics in hafnium silicate films using MOS capacitance transients. Microelectronic Engineering, 2007, 84, 2390-2393.	2.4	3
108	An Assessment of the Location of As-Grown Electron Traps in$hboxHfO_2$/HfSiO Stacks. IEEE Electron Device Letters, 2006, 27, 817-820.	3.9	35

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109	Electrical signature of the defect associated with gate oxide breakdown. IEEE Electron Device Letters, 2006, 27, 393-395.	3.9	19
110	Determination of capture cross sections for as-grown electron traps in HfO2âˆ•HfSiO stacks. Journal of Applied Physics, 2006, 100, 093716.	2.5	41
111	Assessment of capture cross sections and effective density of electron traps generated in silicon dioxides. IEEE Transactions on Electron Devices, 2006, 53, 1347-1354.	3.0	30
112	Impact of gate materials on positive charge formation in HfO2âˆ•SiO2 stacks. Applied Physics Letters, 2006, 89, 023507.	3.3	17
113	Properties and dynamic behavior of electron traps in HfO2/SiO2 stacks. Microelectronic Engineering, 2005, 80, 366-369.	2.4	33
114	Effects of hydrogen on positive charges in gate oxides. Journal of Applied Physics, 2005, 97, 073703.	2.5	29
115	On the role of hydrogen in hole-induced electron trap creation. Semiconductor Science and Technology, 2004, 19, 1333-1338.	2.0	4
116	Hole trap generation in gate dielectric during substrate hole injection. Semiconductor Science and Technology, 2004, 19, L1-L3.	2.0	13
117	Hole Traps in Silicon Dioxidesâ€”Part I: Properties. IEEE Transactions on Electron Devices, 2004, 51, 1267-1273.	3.0	126
118	Hole-Traps in Silicon Dioxidesâ€”Part II: Generation Mechanism. IEEE Transactions on Electron Devices, 2004, 51, 1274-1280.	3.0	36
119	Analysis of the kinetics for interface state generation following hole injection. Journal of Applied Physics, 2003, 93, 6107-6116.	2.5	21
120	Two types of neutral electron traps generated in the gate silicon dioxide. IEEE Transactions on Electron Devices, 2002, 49, 1868-1875.	3.0	33
121	Relation between hole traps and hydrogenous species in silicon dioxides. Solid-State Electronics, 2002, 46, 1839-1847.	1.4	20
122	Relation between hole traps and non-reactive hydrogen-induced positive charges. Microelectronic Engineering, 2001, 59, 67-72.	2.4	0
123	On the mechanism of electron trap generation in gate oxides. Microelectronic Engineering, 2001, 59, 89-94.	2.4	8
124	Dependence of energy distributions of interface states on stress conditions. Microelectronic Engineering, 2001, 59, 95-99.	2.4	2
125	Hole trapping and trap generation in the gate silicon dioxide. IEEE Transactions on Electron Devices, 2001, 48, 1127-1135.	3.0	63
126	Generation of mobile hydrogenous ions in gate oxide and their potential applications. Electronics Letters, 2001, 37, 716.	1.0	3

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127	Degradation of oxides and oxynitrides under hot hole stress. IEEE Transactions on Electron Devices, 2000, 47, 378-386.	3.0	26
128	Still image compression based on 2D discrete wavelet transform. Electronics Letters, 1999, 35, 1934.	1.0	1
129	Relation between hydrogen and the generation of interface state precursors. Microelectronic Engineering, 1999, 48, 135-138.	2.4	4
130	Positive bias temperature instability in MOSFETs. IEEE Transactions on Electron Devices, 1998, 45, 116-124.	3.0	70
131	Generation and annealing of hot hole induced interface states. Microelectronic Engineering, 1997, 36, 227-230.	2.4	1
132	On the hot hole induced post-stress interface trap generation in MOSFET's. , 1996, , .		5
133	Effects of high field injection on the hot carrier induced degradation of submicrometer pMOSFET's. IEEE Transactions on Electron Devices, 1995, 42, 1269-1276.	3.0	18
134	Plasma oxidation of Si and SiGe. Microelectronic Engineering, 1995, 28, 221-224.	2.4	3
135	Donor-like interface trap generation in pMOSFET's at room temperature. IEEE Transactions on Electron Devices, 1994, 41, 740-744.	3.0	11
136	Interface quality of SiGe oxide prepared by RF plasma anodisation. Electronics Letters, 1994, 30, 1988-1989.	1.0	21
137	Recovery of submicrometre pMOSFETs from hot carrier degradation by high field injection. Electronics Letters, 1993, 29, 1097.	1.0	0
138	Microscopy of plasma anodised materials for VLSI. Proceedings Annual Meeting Electron Microscopy Society of America, 1990, 48, 632-633.	0.0	0
139	Interface state behaviour of plasma grown oxides following low temperature annealing. Applied Surface Science, 1989, 39, 374-380.	6.1	11
140	Assessment of plasma-grown oxides on Si:Ge substrates. Applied Surface Science, 1989, 39, 57-64.	6.1	18
141	Dynamic behavior of high-pressure arcs near the flow stagnation point. IEEE Transactions on Plasma Science, 1989, 17, 524-533.	1.3	15
142	Low-temperature gate dielectrics formed by plasma anodisation of silicon nitride. Electronics Letters, 1988, 24, 1269.	1.0	11
143	The computation of self-similar arcs. Computer Physics Communications, 1987, 47, 267-280.	7.5	3
144	A comparative study of positive and negative bias temperature instabilities in MOSFETs. , 0, , .		0

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145	Hydrogen induced and plasma charging enhanced positive charge generation in gate oxides. , 0, , .		2
146	MOSFETs reliability: electron trapping in gate dielectric. , 0, , .		2
147	Generation of hole traps in silicon dioxides. , 0, , .		1
148	A review of positive charge formation in gate oxides. , 0, , .		1
149	A comparative study of positive and negative bias temperature instabilities in MOSFETs. , 0, , .		0