Wenjian Yu

List of Publications by Year in Descending Order

102 papers	1,433 citations	18 h-index	35 g-index
145 ext. papers	1,756 ext. citations	2.4 avg, IF	4.58 L-index

#	Paper	IF	Citations
102	DP-Nets: Dynamic programming assisted quantization schemes for DNN compression and acceleration. *The Integration VLSI Journal*, **2022**, 82, 147-154	1.4	0
101	Faster tensor train decomposition for sparse data. *Journal of Computational and Applied Mathematics*, **2021**, 405, 113972	2.4	1
100	Fast Physics-Based Electromigration Analysis for Full-Chip Networks by Efficient Eigenfunction-Based Solution. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 507-520	2.5	1
99	Efficient and Accuracy-Ensured Waveform Compression for Transient Circuit Simulation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1437-1449	2.5	1
98	feGRASS: Fast and Effective Graph Spectral Sparsification for Scalable Power Grid Analysis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	0
97	Dynamic Programming Assisted Quantization Approaches for Compressing Normal and Robust DNN Models **2021**,		3
96	Advancements and Challenges on Parasitic Extraction for Advanced Process Technologies **2021**,		2
95	Volume Reduction and Fast Generation of the Pre-Characterization Data for Floating Random Walk Based Capacitance Extraction. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	1
94	Fast and Accurate Tensor Completion With Total Variation Regularized Tensor Trains. *IEEE Transactions on Image Processing*, **2020**, 29, 6918-6931	8.7	10
93	Floating Random Walk Capacitance Solver Tackling Conformal Dielectric With On-the-Fly Sampling on Eight-Octant Transition Cubes. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 4935-4943	2.5	4
92	Efficient Model-Based Collaborative Filtering with Fast Adaptive PCA **2020**,		1
91	Reliable Macromodel Generation for the Capacitance Extraction Based on Macromodel-Aware Random Walk Algorithm. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 946-951	2.5	3
90	Machine-Learning-Driven Matrix Ordering for Power Grid Analysis **2019**,		2
89	Realizing Reproducible and Reusable Parallel Floating Random Walk Solvers for Practical Usage **2019**,		2
88	A Unified Approximation Framework for Compressing and Accelerating Deep Neural Networks **2019**,		4
87	Revisiting Kac's method: A Monte Carlo algorithm for solving the Telegrapher's equations. *Mathematics and Computers in Simulation*, **2019**, 156, 178-193	3.3	3
86	Floating Random Walk-Based Capacitance Simulation Considering General Floating Metals. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1711-1715	2.5	7

85	Computing Low-Rank Approximations of Large-Scale Matrices with the Tensor Network Randomized SVD. *SIAM Journal on Matrix Analysis and Applications*, **2018**, 39, 1221-1244	1.5	15
84	Faster Matrix Completion Using Randomized SVD **2018**,		7
83	Fast Training and Model Compression of Gated RNNs via Singular Value Decomposition **2018**,		2
82	Efficient Randomized Algorithms for the Fixed-Precision Low-Rank Matrix Approximation. *SIAM Journal on Matrix Analysis and Applications*, **2018**, 39, 1339-1359	1.5	22
81	Floating Random Walk-Based Capacitance Extraction for General Non-Manhattan Conductor Structures. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 120-133	2.5	8
80	Demand-Side Management of Domestic Electric Water Heaters Using Approximate Dynamic Programming. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 775-788	2.5	29
79	Single-Pass PCA of Large High-Dimensional Data **2017**,		9
78	Improved pre-characterization method for the random walk based capacitance extraction of multi-dielectric VLSI interconnects. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, **2016**, 29, 21-34	1	6
77	Simulation Algorithms With Exponential Integration for Time-Domain Analysis of Large-Scale Power Delivery Networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1681-1694	2.5	11
76	Utilizing macromodels in floating random walk based capacitance extraction **2016**,		4
75	Applications of Monte Carlo method to 3-D capacitance calculation and large matrix decomposition **2016**,		1
74	The application of boundary element method to the resistance calculation problem in designing flat panel displays. *Journal of the Society for Information Display*, **2016**, 24, 177-186	2.1	1
73	A Parallel Random Walk Solver for the Capacitance Calculation Problem in Touchscreen Design **2016**,		8
72	An algorithmic framework for efficient large-scale circuit simulation using exponential integrators **2015**,		4
71	Parallel Thermal Analysis of 3-D Integrated Circuits With Liquid Cooling on CPU-GPU Platforms. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 575-579	2.6	10
70	An efficient method for comprehensive modeling and parasitic extraction of cylindrical through-silicon vias in 3D ICs. *Journal of Semiconductors*, **2015**, 36, 085006	2.3	2
69	Fast Random Walk Based Capacitance Extraction for the 3-D IC Structures With Cylindrical Inter-Tier-Vias. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 1977-1990	2.5	16
68	Ultra-sensitive graphene strain sensor for sound signal acquisition and recognition. *Nano Research*, **2015**, 8, 1627-1636	10	112

67	Efficient techniques for the capacitance extraction of chip-scale VLSI interconnects using floating random walk algorithm **2014**,		19
66	A hybrid random walk algorithm for 3-D thermal analysis of integrated circuits **2014**,		3
65	Random walk based capacitance extraction for 3D ICs with cylindrical inter-tier-vias **2014**,		3
64	The 2-D boundary element techniques for capacitance extraction of nanometer VLSI interconnects. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, **2014**, 27, 656-668	1	12
63	Advanced Field-Solver Techniques for RC Extraction of Integrated Circuits **2014**,		23
62	Process Variation-Aware Capacitance Extraction **2014**, 121-152		
61	FRW-Based Solver for Chip-Scale Large Structures **2014**, 209-231		
60	Statistical Capacitance Extraction Based on Continuous-Surface Geometric Model **2014**, 153-178		
59	Substrate Resistance Extraction with Boundary Element Method **2014**, 91-106		
58	Fast Boundary Element Methods for Capacitance Extraction (I) **2014**, 19-37		0
57	Basic Field-Solver Techniques for RC Extraction **2014**, 7-18		
56	Resistance Extraction of Complex 3-D Interconnects **2014**, 71-89		
55	Extracting Frequency-Dependent Substrate Parasitics **2014**, 107-119		
54	Fast Boundary Element Methods for Capacitance Extraction (II) **2014**, 39-70		
53	Fast Floating Random Walk Method for Capacitance Extraction **2014**, 179-208		
52	Efficient Space Management Techniques for Large-Scale Interconnect Capacitance Extraction With Floating Random Walks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 1633-1637	2.5	30
51	RWCap2: Advanced floating random walk solver for the capacitance extraction of VLSI interconnects **2013**,		4
50	Fast 3-D Thermal Simulation for Integrated Circuits With Domain Decomposition Method. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 2014-2018	2.5	10

49	RWCap: A Floating Random Walk Solver for 3-D Capacitance Extraction of Very-Large-Scale Integration Interconnects. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 353-366	2.5	62
48	Accelerated floating random walk algorithm for the electrostatic computation with 3-D rectilinear-shaped conductors. *Simulation Modelling Practice and Theory*, **2013**, 34, 20-36	3.9	9
47	A 3-D parasitic extraction flow for the modeling and timing analysis of FinFET structures **2013**,		2
46	GPU-friendly floating random walk algorithm for capacitance extraction of VLSI interconnects **2013** ,		24
45	Efficient statistical capacitance extraction of nanometer interconnects considering the on-chip line edge roughness. *Microelectronics Reliability*, **2012**, 52, 704-710	1.2	24
44	Fast floating random walk algorithm formulti-dielectric capacitance extraction with numerical characterization of Green's functions **2012**,		7
43	Statistical extraction and modeling of inductance considering spatial correlation. *Analog Integrated Circuits and Signal Processing*, **2012**, 73, 3-11	1.2	2
42	Stretchable and highly sensitive graphene-on-polymer strain sensors. *Scientific Reports*, **2012**, 2, 870	4.9	450
41	Analysis and Optimization of Low-Power Passive Equalizers for CPUMemory Links. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2011**, 1, 1406-1420	1.7	4
40	Efficient floating random walk algorithm for interconnect capacitance extraction considering multiple dielectrics **2011**,		9
39	Parallel statistical capacitance extraction of on-chip interconnects with an improved geometric variation model **2011**,		12
38	A parasitic extraction method of VLSI interconnects for pre-route timing analysis **2010**,		1
37	Variational Capacitance Extraction and Modeling Based on Orthogonal Polynomial Method. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1556-1566	2.6	17
36	Statistical extraction and modeling of 3-D inductance with spatial correlation **2010**,		2
35	Efficient Power Network Analysis with Modeling of Inductive Effects. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2010**, E93-A, 1196-1203	0.4	1
34	Variational capacitance extraction of on-chip interconnects based on continuous surface model **2009**,		18
33	Efficient power network analysis with complete inductive modeling **2009**,		1
32	Reliability aware through silicon via planning for 3D stacked ICs **2009**,		11

31	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2009**, 28, 1348-1358	2.5	4
30	Accurate Eye Diagram Prediction Based on Step Response and Its Aication to Low-Power Equalizer Design. *IEICE Transactions on Electronics*, **2009**, E92-C, 444-452	0.4	11
29	Efficient Partial Reluctance Extraction for Large-Scale Regular Power Grid Structures. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2009**, E92-A, 1476-1484	0.4	1
28	Efficient Extraction of Frequency-Dependent Substrate Parasitics Using Direct Boundary Element Method. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 1508-1513	2.5	16
27	Low Power Passive Equalizer Design for Computer Memory Links **2008**,		6
26	Clock Skew Analysis via Vector Fitting in Frequency Domain **2008**,		4
25	Efficient frequency-dependent reluctance extraction for large-scale Power/Ground grid **2008**,		1
24	Variational capacitance modeling using orthogonal polynomial method **2008**,		8
23	An efficient method for chip-level statistical capacitance extraction considering process variations with spatial correlation **2008**,		7
22	Low power passive equalizer optimization using tritonic step response **2008**,		6
21	Efficient and accurate eye diagram prediction for high speed signaling **2008**,		21
20	An Efficient Method for Chip-Level Statistical Capacitance Extraction Considering Process Variations with Spatial Correlation **2008**,		12
19	Fast multi-frequency extraction of 3D impedance based on boundary element method. *Microwave and Optical Technology Letters*, **2008**, 50, 2191-2197	1.2	4
18	A mixed surface integral formulation for frequency-dependent inductance calculation of 3D interconnects. *Engineering Analysis With Boundary Elements*, **2007**, 31, 812-818	2.6	2
17	Analytical frequency-dependent model for transmission lines on RF-CMOS lossy substrates. *Tsinghua Science and Technology*, **2007**, 12, 752-756	3.4	
16	Efficient Thermal via Planning Approach and Its Application in 3-D Floorplanning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 645-658	2.5	24
15	Efficient 3-d capacitance extraction considering lossy substrate with multilayered green's function. *IEEE Transactions on Microwave Theory and Techniques*, **2006**, 54, 2128-2137	4.1	11
14	A new boundary element method for accurate modeling of lossy substrates with arbitrary doping profiles **2006**,		12

13	An efficient algorithm for 3-D reluctance extraction considering high frequency effect **2006**,		3
12	Hierarchical H-Adaptive Computation of VLSI Interconnect Capacitance with QMM Acceleration **2006**,		1
11	An Incremental Boundary Element Method for the Variation-Aware Library-Building Procedure of Capacitance Extraction **2006**,		11
10	Efficient 3-D extraction of interconnect capacitance considering floating metal fills with boundary element method. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2006**, 25, 12-18	2.5	29
9	Efficient Direct Boundary Element Method for Resistance Extraction of Substrate With Arbitrary Doping Profile. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2006**, 25, 3035-3042	2.5	16
8	Application of the complete multiple reciprocity method for 3D impedance extraction with multiple frequency points. *Engineering Analysis With Boundary Elements*, **2006**, 30, 640-649	2.6	2
7	Enhanced QMM-BEM solver for three-dimensional multiple-dielectric capacitance extraction within the finite domain. *IEEE Transactions on Microwave Theory and Techniques*, **2004**, 52, 560-566	4.1	41
6	Preconditioned multi-zone boundary element analysis for fast 3D electric simulation. *Engineering Analysis With Boundary Elements*, **2004**, 28, 1035-1044	2.6	20
5	Hierarchical block boundary-element method (HBBEM): a fast field solver for 3-D capacitance extraction. *IEEE Transactions on Microwave Theory and Techniques*, **2004**, 52, 10-19	4.1	26
4	A fast quasi-multiple medium method for 3-D bem calculation of parasitic capacitance. *Computers and Mathematics With Applications*, **2003**, 45, 1883-1894	2.7	11
3	Fast capacitance extraction of actual 3-D VLSI interconnects using quasi-multiple medium accelerated BEM. *IEEE Transactions on Microwave Theory and Techniques*, **2003**, 51, 109-119	4.1	36
2	Substrate resistance extraction with direct boundary element method		1
1	Capacitance Extraction		2