Ingo Sander

List of Publications by Year in descending order

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58 papers	292 citations	1478505 6 h-index	1372567 10 g-index
61 all docs	61 docs citations	61 times ranked	183 citing authors

#	Article	IF	Citations
1	An automated parallel simulation flow for cyber-physical system design. The Integration VLSI Journal, 2021, 77, 48-58.	2.1	2
2	Formulation of Design Space Exploration Problems by Composable Design Space Identification. , 2021, , .		3
3	ForSyDe-Atom. Transactions on Embedded Computing Systems, 2021, 20, 1-27.	2.9	0
4	Classification and Mapping of Model Elements for Designing Runtime Reconfigurable Systems. IEEE Access, 2021, 9, 156337-156360.	4.2	2
5	Heterogeneous co-simulation for embedded and cyber-physical systems design. Simulation, 2020, 96, 753-765.	1.8	3
6	Formal Design, Co-Simulation and Validation of a Radar Signal Processing System. , 2019, , .		4
7	Modeling and Simulation of Dynamic Applications Using Scenario-Aware Dataflow. ACM Transactions on Design Automation of Electronic Systems, 2019, 24, 1-29.	2.6	6
8	Flexible and Tradeoff-Aware Constraint-Based Design Space Exploration for Streaming Applications on Heterogeneous Platforms. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-26.	2.6	9
9	An algebra for modeling continuous time systems. , 2018, , .		1
10	Bridging discrete and continuous time models with atoms. , 2018, , .		1
11	Exploring Power and Throughput for Dataflow Applications on Predictable NoC Multiprocessors. , 2018, , .		8
12	Throughput Propagation in Constraint-Based Design Space Exploration for Mixed-Criticality Systems. , 2017, , .		14
13	CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties. Microprocessors and Microsystems, 2017, 51, 39-55.	2.8	12
14	A layered formal framework for modeling of cyber-physical systems. , 2017, , .		7
15	SAFEPOWER project: Architecture for safe and power-efficient mixed-criticality systems. Microprocessors and Microsystems, 2017, 52, 89-105.	2.8	17
16	ForSyDe: System Design Using a Functional Language and Models of Computation. , 2017, , 99-140.		2
17	Automatic construction of models for analytic system-level design space exploration problems. , 2017, , .		2
18	Designing end-to-end resource reservations in predictable distributed embedded systems. Real-Time Systems, 2017, 53, 916-956.	1.3	10

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19	A modular design space exploration framework for multiprocessor real-time systems. , 2016, , .		8
20	An extensible modeling methodology for embedded and cyber-physical system design. Simulation, 2016, 92, 771-794.	1.8	10
21	SAFEPOWER Project: Architecture for Safe and Power-Efficient Mixed-Criticality Systems. , 2016, , .		6
22	CONTREX: Design of Embedded Mixed-Criticality CONTRol Systems under Consideration of EXtra-Functional Properties. , 2016, , .		4
23	ForSyDe: System Design Using a Functional Language and Models of Computation. , 2016, , 1-42.		4
24	Integrating Functional Mock-up units into a formal heterogeneous system modeling framework. , 2015, , .		0
25	A formal, model-driven design flow for system simulation and multi-core implementation. , 2015, , .		1
26	Towards cognitive reconfigurable hardware: Self-aware learning in RTR fault-tolerant SoCs. , 2015, , .		2
27	Automatic Generation of Virtual Prototypes from Platform Templates. Lecture Notes in Electrical Engineering, 2015, , 147-166.	0.4	1
28	A constraint-based design space exploration framework for real-time applications on MPSoCs. , 2014, , .		6
29	An extensible infrastructure for modeling and time analysis of predictable embedded systems. , 2014, , .		2
30	Synthesizing code for GPGPUs from abstract formal models. , 2014, , .		2
31	On providing scalable self-healing adaptive fault-tolerance to RTR SoCs. , 2014, , .		3
32	The upset-fault-observer: A concept for self-healing adaptive fault tolerance. , 2014, , .		6
33	A constraint-based design space exploration framework for real-time applications on MPSoCs. , 2014, , .		10
34	Towards a Modelling and Design Framework for Mixed-Criticality SoCs and Systems-of-Systems. , 2013, , .		4
35	The RecoBlock SoC Platform: A Flexible Array of Reusable Run-Time-Reconfigurable IP-Blocks. , 2013, , .		6
36	Towards the generic reconfigurable accelerator: Algorithm development, core design, and performance analysis. , 2013, , .		4

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37	System level synthesis of hardware for DSP applications using pre-characterized function implementations. , 2013, , .		3
38	Performance Analysis of Reconfigurations in Adaptive Real-Time Streaming Applications. Transactions on Embedded Computing Systems, 2012, 11S, 1-20.	2.9	1
39	Heterogeneous system-level modeling for small and medium enterprises. , 2012, , .		0
40	Co-simulation of embedded systems in a heterogeneous MoC-based modeling framework. , 2011, , .		7
41	Pareto efficient design for reconfigurable streaming applications on CPU/FPGAs. , 2010, , .		1
42	Constrained global scheduling of streaming applications on MPSoCs. , 2010, , .		11
43	Inferring energy and performance cost of RTOS in priority-driven scheduling. , 2010, , .		1
44	High-level estimation and trade-off analysis for adaptive real-time systems. , 2009, , .		4
45	Implementation of a scalable, globally plesiochronous locally synchronous, off-chip NoC communication protocol. , 2009, , .		3
46	Camera and LCM IP-Cores for NIOS SOPC system. , 2009, , .		0
47	Design and implementation of a plesiochronous multi-core 4x4 network-on-chip FPGA platform with MPI HAL support. , 2009, , .		8
48	Modelling Adaptive Systems in ForSyDe. Electronic Notes in Theoretical Computer Science, 2008, 200, 39-54.	0.9	14
49	Application and Verification of Local Nonsemantic-Preserving Transformations in System Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1091-1103.	2.7	7
50	Performance analysis of reconfiguration in adaptive real-time streaming applications. , 2008, , .		5
51	Energy efficient streaming applications with guaranteed throughput on MPSoCs. , 2008, , .		17
52	Synchronization after design refinements with sensitive delay elements. , 2007, , .		1
53	A synchronization algorithm for local temporal refinements in perfectly synchronous models with nested feedback loops. , 2007, , .		2
54	Using Synchronizers for Refining Synchronous Communication onto Hardware/Software Architectures. Proceedings of the International Workshop on Rapid System Prototyping, 2007, , .	0.0	0

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55	Refining Synchronous Communication onto Network-on-Chip Best-Effort Services. , 2006, , 23-38.		0
56	Verification of design decisions in ForSyDe. , 2003, , .		3
57	A case study of hardware and software synthesis in ForSyDe. , 2002, , .		11
58	The usage of stochastic processes in embedded system specifications. , 2001, , .		6