Meng-Hsueh Chiang

List of Publications by Year
in descending order

40 papers	714 citations	840776 11 h-index	642732 23 g-index
40 all docs	40 docs citations	40 times ranked	1046 citing authors

#	Article	IF	Citations
1	Thinnest Nonvolatile Memory Based on Monolayer hâ€B N. Advanced Materials, 2019, 31, e1806790.	21.0	174
2	Observation of single-defect memristor in an MoS2 atomic sheet. Nature Nanotechnology, 2021, 16, 58-62.	31.5	148
3	Random Dopant Fluctuation in Limited-Width FinFET Technologies. IEEE Transactions on Electron Devices, 2007, 54, 2055-2060.	3.0	116
4	GAAFET Versus Pragmatic FinFET at the 5nm Si-Based CMOS Technology Node. IEEE Journal of the Electron Devices Society, 2017, 5, 164-169.	2.1	54
5	Simulation-Based Study of Hybrid Fin/Planar LDMOS Design for FinFET-Based System-on-Chip Technology. IEEE Transactions on Electron Devices, 2017, 64, 4193-4199.	3.0	25
6	TiO₂-Dielectric AlGaN/GaN/Si Metal-Oxide-Semiconductor High Electron Mobility Transistors by Using Nonvacuum Ultrasonic Spray Pyrolysis Deposition. IEEE Electron Device Letters, 2014, 35, 1091-1093.	3.9	23
7	Investigation of Temperature-Dependent Characteristics of AlGaN/GaN MOS-HEMT by Using Hydrogen Peroxide Oxidation Technique. IEEE Transactions on Electron Devices, 2014, 61, 2760-2766.	3.0	23
8	Design of Gate-All-Around Silicon MOSFETs for 6-T SRAM Area Efficiency and Yield. IEEE Transactions on Electron Devices, 2014, 61, 2371-2377.	3.0	16
9	Variation-Aware Comparative Study of 10-nm GAA Versus FinFET 6-T SRAM Performance and Yield. IEEE Transactions on Electron Devices, 2014, 61, 3949-3954.	3.0	15
10	Integration of Gate Recessing and <italic>In Situ</italic> Cl^{â^'} Doped Al₂O₃ for Enhancement-Mode AlGaN/GaN MOSHEMTs Fabrication. IEEE Electron Device Letters, 2017, 38, 91-94.	3.9	14
11	Atomristors: Memory Effect in Atomically-thin Sheets and Record RF Switches. , 2018, , .		14
12	Stack Gate Technique for Dopingless Bulk FinFETs. IEEE Transactions on Electron Devices, 2014, 61, 963-968.	3.0	12
13	Growing Al₂O₃by Ultrasonic Spray Pyrolysis for Al₂O₃/AlGaN/GaN Metal-Insulator-Semiconductor Ultraviolet Photodetectors. IEEE Transactions on Electron Devices, 2014, 61, 4062-4069.	3.0	9
14	A Predictive Compact Model of Bipolar RRAM Cells for Circuit Simulations. IEEE Transactions on Electron Devices, 2015, 62, 2176-2183.	3.0	8
15	Subthreshold Kink Effect Revisited and Optimized for Si Nanowire MOSFETs. IEEE Transactions on Electron Devices, 2016, 63, 903-909.	3.0	8
16	All-zigzag graphene nanoribbons for planar interconnect application. Journal of Applied Physics, 2017, 122, .	2.5	8
17	Threshold-voltage variability analysis and modeling for junctionless double-gate transistors. Microelectronics Reliability, 2017, 74, 22-26.	1.7	7
18	Insights to the Scaling Impact on Back-Gate Biasing for FD SOI MOSFETs. , 2018, , .		4

#	Article	IF	Citations
19	Multi-threshold design methodology of stacked Si-nanowire FETs. , 2014, , .		3
20	An FET With a Source Tunneling Barrier Showing Suppressed Short-Channel Effects for Low-Power Applications. IEEE Transactions on Electron Devices, 2018, 65, 855-859.	3.0	3
21	An RRAM with a 2D Material Embedded Double Switching Layer for Neuromorphic Computing. , 2018, , .		3
22	Speed Optimization of Vertically Stacked Gate-All-Around MOSFETs with Inner Spacers for Low Power and Ultra-Low Power Applications. , 2019, , .		3
23	Simulation-Based Study of High-Density SRAM Voltage Scaling Enabled by Inserted-Oxide FinFET Technology. IEEE Transactions on Electron Devices, 2019, 66, 1754-1759.	3.0	3
24	Simulation-Based Study of Low Minimum Operating Voltage SRAM With Inserted-Oxide FinFETs and Gate-All-Around Transistors. IEEE Transactions on Electron Devices, 2022, 69, 1823-1829.	3.0	3
25	Comparison of 10 nm GAA vs. FinFET 6-T SRAM performance and yield. , 2014, , .		2
26	6-T SRAM performance assessment with stacked silicon nanowire MOSFETs. , 2015, , .		2
27	An area efficient gate-all-around ring MOSFET. , 2016, , .		2
28	An area efficient low-voltage 6-T SRAM cell using stacked silicon nanowires. , 2018, , .		2
29	Bilayer Modulation With Dual Vacancy Filaments by Intentionally Oxidized Titanium Oxide for Multilayer-hBN RRAM. IEEE Nanotechnology Magazine, 2021, 20, 687-694.	2.0	2
30	Simulation-Based Study of High-Permittivity Inserted-Oxide FinFET With Low-Permittivity Inner Spacers. IEEE Transactions on Electron Devices, 2021, 68, 5529-5534.	3.0	2
31	Performance evaluation of stacked gate-all-around MOSFETs at 7 and 10 nm technology nodes. , 2016, , .		1
32	Gate structure engineering for enhancement-mode AlGaN/GaN MOSHEMT. , 2017, , .		1
33	S-shaped gate-all-around MOSFETs for high density design. , 2017, , .		1
34	High-density SRAM voltage scaling enabled by inserted-oxide FinFET technology. , 2017, , .		1
35	Modeling of RRAM With Embedded Tunneling Barrier and Its Application in Logic in Memory. IEEE Journal of the Electron Devices Society, 2020, 8, 1390-1396.	2.1	1
36	TCAD-Based Assessment of the Lateral GAA Nanosheet Transistor for Future CMOS. IEEE Transactions on Electron Devices, 2021, 68, 6586-6591.	3.0	1

#	Article	IF	Citations
37	An Analytical Gate-All-Around MOSFET Model for Circuit Simulation. Advances in Materials Science and Engineering, 2015, 2015, 1-5.	1.8	0
38	Body-biasing assisted vmin optimization for 5nm-node multi-Vt FD-SOI 6T-SRAM. , 2018, , .		0
39	Gradual RESET modulation by intentionally oxidized titanium oxide for multilayer-hBN RRAM. , 2019, , .		0
40	Back-Bias Modulated UTBB SOI for System-on-Chip I/O Cells. , 2021, , .		0