Jinhui Wang

List of Publications by Year
in descending order

32 papers	204 citations	1162367 8 h-index	1199166 12 g-index
33 all docs	33 docs citations	33 times ranked	142 citing authors

#	ARTICLE	IF	CITATIONS
1	Level Scaling and Pulse Regulating to Mitigate the Impact of the Cycle-to-Cycle Variation in Memristor-Based Edge AI System. IEEE Transactions on Electron Devices, 2022, 69, 1752-1762.	1.6	9
2	Mapping Transformation Enabled High-Performance and Low-Energy Memristor-Based DNNs. Journal of Low Power Electronics and Applications, 2022, 12, 10.	1.3	5
3	Pulse Truncation Enabled High Performance and Low Energy Memristor-based Accelerator. , 2022, , .		1
4	Memristor-Based Variation-Enabled Differentially Private Learning Systems for Edge Computing in IoT. IEEE Internet of Things Journal, 2021, 8, 9672-9682.	5.5	8
5	Ameliorate Performance of Memristor-Based ANNs in Edge Computing. IEEE Transactions on Computers, 2021, 70, 1299-1310.	2.4	11
6	Cycle-to-cycle Variation Enabled Energy Efficient Privacy Preserving Technology in ANN. , 2020, , .		3
7	Memristor-Based Neuromorphic Hardware Improvement for Privacy-Preserving ANN. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2745-2754.	2.1	14
8	Linear Optimization for Memristive Device in Neuromorphic Hardware. , 2019, , .		7
9	Content-Adaptive Memory for Viewer-Aware Energy-Quality Scalable Mobile Video Systems. IEEE Access, 2019, 7, 47479-47493.	2.6	8
10	Mitigating Nonlinear Effect of Memristive Synaptic Device for Neuromorphic Computing. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 377-387.	2.7	27
11	Data-Pattern Enabled Self-Recovery Low-Power Storage System for Big Video Data. IEEE Transactions on Big Data, 2019, 5, 95-105.	4.4	12
12	Viewer-Aware Intelligent Efficient Mobile Video Embedded Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 684-696.	2.1	9
13	A Novel Hybrid Delay Unit Based on Dummy TSVs for 3-D On-Chip Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1277-1289.	2.1	1
14	SPIDER: Sizing-Priority-Based Application-Driven Memory for Mobile Video Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2625-2634.	2.1	7
15	Closed form delay models for buffer-driven TSVs in 3D on-chip memory. , 2017, , .		0
16	TSV modelling in 3D IC thermoelectric simulation. , 2017, , .		1
17	Data-Driven Intelligent Efficient Synaptic Storage for Deep Learning. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1412-1416.	2.2	6
18	On-chip thermal management method based on phase change material. , 2017, , .		1

#	Article	IF	Citations
19	Dummy TSV based bit-line optimization in 3D on-chip memory. , 2016, , .		2
20	3D memory design based on through silicon vias enabled timing optimization. , 2016, , .		0
21	RF-powered battery-less Wireless Sensor Network. , 2016, , .		4
22	Platform design for compatible semi-custom design flow. , 2016, , .		0
23	MTJ based data restoration in non-volatile SRAM. , 2016, , .		2
24	Sizing-priority based low-power embedded memory for mobile video applications. , 2016, , .		12
25	PNS-FCR: Flexible Charge Recycling Dynamic Circuit Technique for Low-Power Microprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 613-624.	2.1	3
26	Luminance-adaptive smart video storage system. , 2016, , .		4
27	VCAS: Viewing context aware power-efficient mobile video embedded memory. , 2015, , .		4
28	TM-RF: Aging-Aware Power-Efficient Register File Design for Modern Microprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1196-1209.	2.1	8
29	Specific MCU design of On board Unit in Electronic Toll Collection system. , 2014, , .		1
30	Variation Aware Sleep Vector Selection in Dual V_{mt} Dynamic OR Circuits for Low Leakage Register File Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1970-1983.	3.5	8
31	CMOS 1.2V bandgap voltage reference design. , 2013, , .		5
32	Low power and high performance dynamic CMOS XOR/XNOR gate design. Microelectronic Engineering, 2011, 88, 2781-2784.	1.1	21