Mohammad Gholami

List of Publications by Citations

50 papers	301 citations	10 h-index	13 g-index
59 ext. papers	425 ext. citations	2.1 avg, IF	4.44 L-index

#	Paper	IF	Citations
50	Phase Detector with Minimal Blind Zone and Reset Time for GSamples/s DLLs. *Circuits, Systems, and Signal Processing*, **2017**, 36, 3549-3563	2.2	16
49	A novel efficient full adder□ubtractor in QCA nanotechnology. *International Nano Letters*, **2019**, 9, 51-54	5.7	16
48	Analysis of frequency and amplitude in CMOS differential ring oscillators. *The Integration VLSI Journal*, **2016**, 52, 253-259	1.4	15
47	Novel D Latches and D Flip-Flops with Set and Reset Ability in QCA Nanotechnology Using Minimum Cells and Area. *International Journal of Theoretical Physics*, **2018**, 57, 3223-3241	1.1	15
46	A novel rising Edge Triggered Resettable D flip-flop using five input majority gate. *Microprocessors and Microsystems*, **2018**, 61, 327-335	2.4	15
45	Using a memristor crossbar structure to implement a novel adaptive real-time fuzzy modeling algorithm. *Fuzzy Sets and Systems*, **2017**, 307, 115-128	3.7	13
44	4-Bit serial shift register with reset ability and 4-bit LFSR in QCA technology using minimum number of cells and delay. *Computers and Electrical Engineering*, **2019**, 78, 449-462	4.3	13
43	A Novel Low Power Architecture for DLL-Based Frequency Synthesizers. *Circuits, Systems, and Signal Processing*, **2013**, 32, 781-801	2.2	13
42	Jitter of Delay-Locked Loops Due to PFD. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 2176-2180	2.6	12
41	A novel architecture for low voltage-low power DLL-based frequency multipliers. *IEICE Electronics Express*, **2011**, 8, 859-865	0.5	11
40	Low-Power High-Frequency Phase Frequency Detector for Minimal Blind-Zone Phase-Locked Loops. *Circuits, Systems, and Signal Processing*, **2019**, 38, 498-511	2.2	10
39	Design of Multiplexer-Based D Flip-Flop with Set and Reset Ability in Quantum Dot Cellular Automata Nanotechnology. *International Journal of Theoretical Physics*, **2019**, 58, 687-699	1.1	10
38	Two Novel Ultra-Low-Power SRAM Cells with Separate Read and Write Path. *Circuits, Systems, and Signal Processing*, **2019**, 38, 287-303	2.2	9
37	All digital fast lock DLL-based frequency multiplier. *Analog Integrated Circuits and Signal Processing*, **2014**, 78, 819-826	1.2	9
36	Counters Designs with Minimum Number of Cells and Area in the Quantum-Dot Cellular Automata Technology. *International Journal of Theoretical Physics*, **2019**, 58, 1758-1775	1.1	8
35	Molecular simulations of adsorption and separation of ethylene/ethane and propylene/propane mixtures on Ni2(dobdc) and Ni2(m-dobdc) metal-organic frameworks. *Molecular Simulation*, **2018**, 44, 389-395	2	8
34	A wide range delay locked loop for low power and low jitter applications. *International Journal of Circuit Theory and Applications*, **2018**, 46, 401-414	2	8

33	Analysis of DLL Jitter due to Voltage-Controlled Delay Line. *Circuits, Systems, and Signal Processing*, **2013**, 32, 2119-2135	2.2	8
32	Parity generator and digital code converter in QCA nanotechnology. *International Nano Letters*, **2020**, 10, 49-59	5.7	8
31	Molecular simulations of adsorption and separation of acetylene and methane and their binary mixture on MOF-5, HKUST-1 and MOF-505 metal–organic frameworks. *Molecular Simulation*, **2017**, 43, 260-266	2	7
30	Design of novel D flip-flops with set and reset abilities in quantum-dot cellular automata nanotechnology. *Computers and Electrical Engineering*, **2019**, 74, 259-272	4.3	7
29	Digital delay locked loop-based frequency synthesiser for Digital Video Broadcasting-Terrestrial receivers. *IET Circuits, Devices and Systems*, **2014**, 8, 38-46	1.1	7
28	A Novel Charge Pump with Low Current for Low-Power Delay-Locked Loops. *Circuits, Systems, and Signal Processing*, **2017**, 36, 3514-3526	2.2	6
27	Low-power and wide-band delay-locked loop with switching delay line. *International Journal of Circuit Theory and Applications*, **2018**, 46, 2189-2201	2	6
26	Low voltage and low power DLL-based frequency synthesizer for covering VHF frequency band **2011**,		6
25	A wide frequency range delay line for fast-locking and low power delay-locked-loops. *Analog Integrated Circuits and Signal Processing*, **2017**, 90, 427-434	1.2	5
24	Adsorption of propylene, propane, ethylene and ethane in an isoreticular series of MOF-74 structures. *Adsorption*, **2017**, 23, 507-514	2.6	4
23	Design of 3.1 to 10.6 GHz ultra-wideband flat gain LNA. *International Journal of Circuit Theory and Applications*, **2017**, 45, 2034-2045	2	4
22	A Low-Power and High-Frequency Phase Frequency Detector for a 3.33-GHz Delay Locked Loop. *Circuits, Systems, and Signal Processing*, **2020**, 39, 1735-1750	2.2	4
21	A new fast-lock, low-jitter, and all-digital frequency synthesizer for DVB-T receivers. *International Journal of Circuit Theory and Applications*, **2015**, 43, 566-578	2	3
20	Compact, low-voltage, low-power and high-bandwidth CMOS four-quadrant analog multiplier **2010**,		3
19	A low-jitter clock multiplier using a simple low-power ECDLL with extra settled delays in VCDL. *Analog Integrated Circuits and Signal Processing*, **2020**, 102, 541-554	1.2	2
18	Design and analysis of high linearity mixer using subharmonic technique. *International Journal of Circuit Theory and Applications*, **2018**, 46, 2202-2216	2	2
17	Increasing frequency of ring oscillators by using negative capacitors. *Electronics Letters*, **2012**, 48, 1109-1110	1.1	2
16	A low power 1-V 10-bit 40-MS/s pipeline ADC **2011**,		2

15	A novel parallel architecture for low voltage-low power DLL-based frequency multiplier **2011**,		2
14	New method to synthesize the frequency bands with DLL-based frequency synthesizer **2011**,		2
13	Using D flip-flop with reset terminal to design PFD in QCA nanotechnology. *International Journal of Electronics*, **2020**, 107, 1940-1962	1.2	2
12	Total Jitter of Delay-Locked Loops Due to Four Main Jitter Sources. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 1-10	2.6	1
11	Design of Novel Testable and Diagnosable Phase-Frequency Detector. *Circuits, Systems, and Signal Processing*, **2014**, 33, 999-1018	2.2	1
10	Covering VHF frequency band with novel DLL-based frequency synthesizer **2011**,		1
9	Modeling of DLL-based frequency multiplier in time and frequency domain with Matlab Simulink **2010**,		1
8	A DLL-based frequency synthesizer for VHF DVB-H/T receivers **2010**,		1
7	Novel quantum-dot cellular automata implementation of flip-flop and phase-frequency detector based on nand-nor-inverter gates. *International Journal of Circuit Theory and Applications*, **2021**, 49, 196-212	2	1
6	Analysis and design of a low jitter delay-locked loop using lock state detector. *International Journal of Circuit Theory and Applications*, **2021**, 49, 1410-1419	2	1
5	Phase-frequency detector in QCA nanotechnology using novel flip-flop with reset terminal. *International Nano Letters*, **2020**, 10, 111-118	5.7	0
4	Overview of Analog Wide Range Delay Locked Loops. *Recent Advances in Electrical and Electronic Engineering*, **2018**, 11, 470-483	0.3	0
3	Analysis and Design of the Pseudo-Random Bit Generator in the Technology of Quantum-Dot Cellular Automata. *International Journal of Theoretical Physics*, **2020**, 59, 29-48	1.1	0
2	Design and analysis of negative capacitor by using MOSFETs. *International Journal of Electronics*, **2014**, 101, 1167-1177	1.2	
1	A low power and jitter delay cell with pulse width modulation for wide range delay lock loops. *Microelectronics Journal*, **2021**, 112, 105054	1.8	