Mohammad Gholami

List of Publications by Year
in descending order

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58	567	623734	752698
papers	citations	14	20
		h-index	g-index

59	59	59	245
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A novel efficient full adderâ€“subtractor in QCA nanotechnology. International Nano Letters, 2019, 9, 51-54.	5.0	33
2	Phase Detector with Minimal Blind Zone and Reset Time for GSamples/s DLLs. Circuits, Systems, and Signal Processing, 2017, 36, 3549-3563.	2.0	30
3	Novel D Latches and D Flip-Flops with Set and Reset Ability in QCA Nanotechnology Using Minimum Cells and Area. International Journal of Theoretical Physics, 2018, 57, 3223-3241.	1.2	30
4	4-Bit serial shift register with reset ability and 4-bit LFSR in QCA technology using minimum number of cells and delay. Computers and Electrical Engineering, 2019, 78, 449-462.	4.8	28
5	A novel rising Edge Triggered Resettable D flip-flop using five input majority gate. Microprocessors and Microsystems, 2018, 61, 327-335.	2.8	24
6	Low-Power High-Frequency Phase Frequency Detector for Minimal Blind-Zone Phase-Locked Loops. Circuits, Systems, and Signal Processing, 2019, 38, 498-511.	2.0	23
7	Parity generator and digital code converter in QCA nanotechnology. International Nano Letters, 2020, 10, 49-59.	5.0	20
8	Two Novel Ultra-Low-Power SRAM Cells with Separate Read and Write Path. Circuits, Systems, and Signal Processing, 2019, 38, 287-303.	2.0	19
9	Counters Designs with Minimum Number of Cells and Area in the Quantum-Dot Cellular Automata Technology. International Journal of Theoretical Physics, 2019, 58, 1758-1775.	1.2	19
10	A Novel Low Power Architecture for DLL-Based Frequency Synthesizers. Circuits, Systems, and Signal Processing, 2013, 32, 781-801.	2.0	18
11	Jitter of Delay-Locked Loops Due to PFD. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2176-2180.	3.1	18
12	Analysis of frequency and amplitude in CMOS differential ring oscillators. The Integration VLSI Journal, 2016, 52, 253-259.	2.1	18
13	Using a memristor crossbar structure to implement a novel adaptive real-time fuzzy modeling algorithm. Fuzzy Sets and Systems, 2017, 307, 115-128.	2.7	17
14	Design of Multiplexer-Based D Flip-Flop with Set and Reset Ability in Quantum Dot Cellular Automata Nanotechnology. International Journal of Theoretical Physics, 2019, 58, 687-699.	1.2	17
15	A Low-Power and High-Frequency Phase Frequency Detector for a 3.33-GHz Delay Locked Loop. Circuits, Systems, and Signal Processing, 2020, 39, 1735-1750.	2.0	17
16	A novel architecture for low voltage-low power DLL-based frequency multipliers. IEICE Electronics Express, 2011, 8, 859-865.	0.8	14
17	Design of novel D flip-flops with set and reset abilities in quantum-dot cellular automata nanotechnology. Computers and Electrical Engineering, 2019, 74, 259-272.	4.8	14
18	All digital fast lock DLL-based frequency multiplier. Analog Integrated Circuits and Signal Processing, 2014, 78, 819-826.	1.4	13

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19	A wide range delay locked loop for low power and low jitter applications. International Journal of Circuit Theory and Applications, 2018, 46, 401-414.	2.0	13
20	Molecular simulations of adsorption and separation of acetylene and methane and their binary mixture on MOF-5, HKUST-1 and MOF-505 metalâ€“organic frameworks. Molecular Simulation, 2017, 43, 260-266.	2.0	12
21	Lowâ€power and wideâ€band delayâ€locked loop with switching delay line. International Journal of Circuit Theory and Applications, 2018, 46, 2189-2201.	2.0	12
22	Analysis of DLL Jitter due to Voltage-Controlled Delay Line. Circuits, Systems, and Signal Processing, 2013, 32, 2119-2135.	2.0	11
23	Digital delay locked loopâ€based frequency synthesiser for Digital Video Broadcastingâ€Terrestrial receivers. IET Circuits, Devices and Systems, 2014, 8, 38-46.	1.4	11
24	Molecular simulations of adsorption and separation of ethylene/ethane and propylene/propane mixtures on Ni2(dobdc) and Ni2(m-dobdc) metal-organic frameworks. Molecular Simulation, 2018, 44, 389-395.	2.0	10
25	A Novel Charge Pump with Low Current for Low-Power Delay-Locked Loops. Circuits, Systems, and Signal Processing, 2017, 36, 3514-3526.	2.0	8
26	Latch and flip-flop design in QCA technology with minimum number of cells. Computers and Electrical Engineering, 2022, 102, 108186.	4.8	8
27	Low voltage and low power DLL-based frequency synthesizer for covering VHF frequency band. , 2011, , .		7
28	A new fastâ€lock, lowâ€jitter, and allâ€digital frequency synthesizer for DVBâ€T receivers. International Journal of Circuit Theory and Applications, 2015, 43, 566-578.	2.0	7
29	Design of 3.1 to 10.6ÂGHz ultraâ€wideband flat gain LNA. International Journal of Circuit Theory and Applications, 2017, 45, 2034-2045.	2.0	7
30	A wide frequency range delay line for fast-locking and low power delay-locked-loops. Analog Integrated Circuits and Signal Processing, 2017, 90, 427-434.	1.4	7
31	Adsorption of propylene, propane, ethylene and ethane in an isoreticular series of MOF-74 structures. Adsorption, 2017, 23, 507-514.	3.0	6
32	Analysis and Design of the Pseudo-Random Bit Generator in the Technology of Quantum-Dot Cellular Automata. International Journal of Theoretical Physics, 2020, 59, 29-48.	1.2	6
33	Phase-frequency detector in QCA nanotechnology using novel flip-flop with reset terminal. International Nano Letters, 2020, 10, 111-118.	5.0	6
34	A low-jitter clock multiplier using a simple low-power ECDLL with extra settled delays in VCDL. Analog Integrated Circuits and Signal Processing, 2020, 102, 541-554.	1.4	6
35	Novel quantumâ€dot cellular automata implementation of flipâ€flop and phaseâ€frequency detector based on nandâ€norâ€inverter gates. International Journal of Circuit Theory and Applications, 2021, 49, 196-212.	2.0	6
36	New method to synthesize the frequency bands with DLL-based frequency synthesizer. , 2011, , .		5

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37	Increasing frequency of ring oscillators by using negative capacitors. Electronics Letters, 2012, 48, 1109-1110.	1.0	5
38	Using D flip-flop with reset terminal to design PFD in QCA nanotechnology. International Journal of Electronics, 2020, 107, 1940-1962.	1.4	5
39	Analysis and design of a low jitter delayâ€locked loop using lock state detector. International Journal of Circuit Theory and Applications, 2021, 49, 1410-1419.	2.0	4
40	Compact, low-voltage, low-power and high-bandwidth CMOS four-quadrant analog multiplier. , 2010, , .		3
41	A low power 1-V 10-bit 40-MS/s pipeline ADC. , 2011, , .		3
42	Total Jitter of Delay-Locked Loops Due to Four Main Jitter Sources. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, , 1-10.	3.1	3
43	A Noise and Mismatches of Delay Cells and Their Effects on DLLs. International Journal of Intelligent Systems and Applications, 2014, 6, 37-43.	1.1	3
44	Modeling of DLL-based frequency multiplier in time and frequency domain with Matlab Simulink. , 2010, , .		2
45	A novel parallel architecture for low voltage-low power DLL-based frequency multiplier. , 2011, , .		2
46	Design of Novel Testable and Diagnosable Phase-Frequency Detector. Circuits, Systems, and Signal Processing, 2014, 33, 999-1018.	2.0	2
47	Design and analysis of high linearity mixer using subharmonic technique. International Journal of Circuit Theory and Applications, 2018, 46, 2202-2216.	2.0	2
48	Dual Phase Detector Based Delay Locked Loop for High Speed Applications. International Journal of Engineering, Transactions B: Applications, 2014, 27, .	0.7	2
49	Phase Frequency Detector Using Transmission Gates for High Speed Applications. International Journal of Engineering, Transactions B: Applications, 2016, 29, .	0.7	2
50	Selective counter design in <scp>quantumâ€dot</scp> cellular automata nanotechnology. Concurrency Computation Practice and Experience, 2022, 34, .	2.2	2
51	Systematic modeling and simulation of DLL-based frequency multiplier. , 2010, , .		1
52	A DLL-based frequency synthesizer for VHF DVB-H/T receivers. , 2010, , .		1
53	Covering VHF frequency band with novel DLL-based frequency synthesizer. , 2011, , .		1
54	Design and analysis of negative capacitor by using MOSFETs. International Journal of Electronics, 2014, 101, 1167-1177.	1.4	1

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55	A low power and jitter delay cell with pulse width modulation for wide range delay lock loops. Microelectronics Journal, 2021, 112, 105054.	2.0	1
56	Low Settling Time All Digital DLL for VHF Application. International Journal of Engineering, Transactions B: Applications, 2015, 28, .	0.7	1
57	Overview of Analog Wide Range Delay Locked Loops. Recent Advances in Electrical and Electronic Engineering, 2018, 11, 470-483.	0.3	1
58	Two Novel Flip Flop with Level Triggered Reset in Quantum Dot Cellular Automata. International Journal of Engineering, Transactions B: Applications, 2018, 31, .	0.7	0