

Mohammad Gholami

List of Publications by Year in descending order

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54
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times ranked

245
citing authors

| # | ARTICLE | IF | CITATIONS |
|----|--|-----|-----------|
| 1 | A novel efficient full adder-subtractor in QCA nanotechnology. <i>International Nano Letters</i> , 2019, 9, 51-54. | 2.3 | 33 |
| 2 | Phase Detector with Minimal Blind Zone and Reset Time for GSamples/s DLLs. <i>Circuits, Systems, and Signal Processing</i> , 2017, 36, 3549-3563. | 1.2 | 30 |
| 3 | Novel D Latches and D Flip-Flops with Set and Reset Ability in QCA Nanotechnology Using Minimum Cells and Area. <i>International Journal of Theoretical Physics</i> , 2018, 57, 3223-3241. | 0.5 | 30 |
| 4 | 4-Bit serial shift register with reset ability and 4-bit LFSR in QCA technology using minimum number of cells and delay. <i>Computers and Electrical Engineering</i> , 2019, 78, 449-462. | 3.0 | 28 |
| 5 | A novel rising Edge Triggered Resettable D flip-flop using five input majority gate. <i>Microprocessors and Microsystems</i> , 2018, 61, 327-335. | 1.8 | 24 |
| 6 | Low-Power High-Frequency Phase Frequency Detector for Minimal Blind-Zone Phase-Locked Loops. <i>Circuits, Systems, and Signal Processing</i> , 2019, 38, 498-511. | 1.2 | 23 |
| 7 | Parity generator and digital code converter in QCA nanotechnology. <i>International Nano Letters</i> , 2020, 10, 49-59. | 2.3 | 20 |
| 8 | Two Novel Ultra-Low-Power SRAM Cells with Separate Read and Write Path. <i>Circuits, Systems, and Signal Processing</i> , 2019, 38, 287-303. | 1.2 | 19 |
| 9 | Counters Designs with Minimum Number of Cells and Area in the Quantum-Dot Cellular Automata Technology. <i>International Journal of Theoretical Physics</i> , 2019, 58, 1758-1775. | 0.5 | 19 |
| 10 | A Novel Low Power Architecture for DLL-Based Frequency Synthesizers. <i>Circuits, Systems, and Signal Processing</i> , 2013, 32, 781-801. | 1.2 | 18 |
| 11 | Jitter of Delay-Locked Loops Due to PFD. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2014, 22, 2176-2180. | 2.1 | 18 |
| 12 | Analysis of frequency and amplitude in CMOS differential ring oscillators. <i>The Integration VLSI Journal</i> , 2016, 52, 253-259. | 1.3 | 18 |
| 13 | Using a memristor crossbar structure to implement a novel adaptive real-time fuzzy modeling algorithm. <i>Fuzzy Sets and Systems</i> , 2017, 307, 115-128. | 1.6 | 17 |
| 14 | Design of Multiplexer-Based D Flip-Flop with Set and Reset Ability in Quantum Dot Cellular Automata Nanotechnology. <i>International Journal of Theoretical Physics</i> , 2019, 58, 687-699. | 0.5 | 17 |
| 15 | A Low-Power and High-Frequency Phase Frequency Detector for a 3.33-GHz Delay Locked Loop. <i>Circuits, Systems, and Signal Processing</i> , 2020, 39, 1735-1750. | 1.2 | 17 |
| 16 | A novel architecture for low voltage-low power DLL-based frequency multipliers. <i>IEICE Electronics Express</i> , 2011, 8, 859-865. | 0.3 | 14 |
| 17 | Design of novel D flip-flops with set and reset abilities in quantum-dot cellular automata nanotechnology. <i>Computers and Electrical Engineering</i> , 2019, 74, 259-272. | 3.0 | 14 |
| 18 | All digital fast lock DLL-based frequency multiplier. <i>Analog Integrated Circuits and Signal Processing</i> , 2014, 78, 819-826. | 0.9 | 13 |

| # | ARTICLE | IF | CITATIONS |
|----|--|-----|-----------|
| 19 | A wide range delay locked loop for low power and low jitter applications. International Journal of Circuit Theory and Applications, 2018, 46, 401-414. | 1.3 | 13 |
| 20 | Molecular simulations of adsorption and separation of acetylene and methane and their binary mixture on MOF-5, HKUST-1 and MOF-505 metal-organic frameworks. Molecular Simulation, 2017, 43, 260-266. | 0.9 | 12 |
| 21 | Low-power and wide-band delay-locked loop with switching delay line. International Journal of Circuit Theory and Applications, 2018, 46, 2189-2201. | 1.3 | 12 |
| 22 | Analysis of DLL Jitter due to Voltage-Controlled Delay Line. Circuits, Systems, and Signal Processing, 2013, 32, 2119-2135. | 1.2 | 11 |
| 23 | Digital delay locked loop-based frequency synthesizer for Digital Video Broadcasting-terrestrial receivers. IET Circuits, Devices and Systems, 2014, 8, 38-46. | 0.9 | 11 |
| 24 | Molecular simulations of adsorption and separation of ethylene/ethane and propylene/propane mixtures on Ni ₂ (dobdc) and Ni ₂ (m-dobdc) metal-organic frameworks. Molecular Simulation, 2018, 44, 389-395. | 0.9 | 10 |
| 25 | A Novel Charge Pump with Low Current for Low-Power Delay-Locked Loops. Circuits, Systems, and Signal Processing, 2017, 36, 3514-3526. | 1.2 | 8 |
| 26 | Latch and flip-flop design in QCA technology with minimum number of cells. Computers and Electrical Engineering, 2022, 102, 108186. | 3.0 | 8 |
| 27 | Low voltage and low power DLL-based frequency synthesizer for covering VHF frequency band. , 2011, , . | | 7 |
| 28 | A new fast-lock, low-jitter, and all-digital frequency synthesizer for DVB-T receivers. International Journal of Circuit Theory and Applications, 2015, 43, 566-578. | 1.3 | 7 |
| 29 | Design of 3.1 to 10.6 GHz ultra-wideband flat gain LNA. International Journal of Circuit Theory and Applications, 2017, 45, 2034-2045. | 1.3 | 7 |
| 30 | A wide frequency range delay line for fast-locking and low power delay-locked-loops. Analog Integrated Circuits and Signal Processing, 2017, 90, 427-434. | 0.9 | 7 |
| 31 | Adsorption of propylene, propane, ethylene and ethane in an isorecticular series of MOF-74 structures. Adsorption, 2017, 23, 507-514. | 1.4 | 6 |
| 32 | Analysis and Design of the Pseudo-Random Bit Generator in the Technology of Quantum-Dot Cellular Automata. International Journal of Theoretical Physics, 2020, 59, 29-48. | 0.5 | 6 |
| 33 | Phase-frequency detector in QCA nanotechnology using novel flip-flop with reset terminal. International Nano Letters, 2020, 10, 111-118. | 2.3 | 6 |
| 34 | A low-jitter clock multiplier using a simple low-power ECDLL with extra settled delays in VCDL. Analog Integrated Circuits and Signal Processing, 2020, 102, 541-554. | 0.9 | 6 |
| 35 | Novel quantum-dot cellular automata implementation of flip-flop and phase-frequency detector based on NAND-inverter gates. International Journal of Circuit Theory and Applications, 2021, 49, 196-212. | 1.3 | 6 |
| 36 | New method to synthesize the frequency bands with DLL-based frequency synthesizer. , 2011, , . | | 5 |

| # | ARTICLE | IF | CITATIONS |
|----|---|-----|-----------|
| 37 | Increasing frequency of ring oscillators by using negative capacitors. Electronics Letters, 2012, 48, 1109-1110. | 0.5 | 5 |
| 38 | Using D flip-flop with reset terminal to design PFD in QCA nanotechnology. International Journal of Electronics, 2020, 107, 1940-1962. | 0.9 | 5 |
| 39 | Analysis and design of a low jitter delay-locked loop using lock state detector. International Journal of Circuit Theory and Applications, 2021, 49, 1410-1419. | 1.3 | 4 |
| 40 | Compact, low-voltage, low-power and high-bandwidth CMOS four-quadrant analog multiplier. , 2010, , | | 3 |
| 41 | A low power 1-V 10-bit 40-MS/s pipeline ADC. , 2011, , . | | 3 |
| 42 | Total Jitter of Delay-Locked Loops Due to Four Main Jitter Sources. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, , 1-10. | 2.1 | 3 |
| 43 | A Noise and Mismatches of Delay Cells and Their Effects on DLLs. International Journal of Intelligent Systems and Applications, 2014, 6, 37-43. | 0.9 | 3 |
| 44 | Modeling of DLL-based frequency multiplier in time and frequency domain with Matlab Simulink. , 2010, , . | | 2 |
| 45 | A novel parallel architecture for low voltage-low power DLL-based frequency multiplier. , 2011, , . | | 2 |
| 46 | Design of Novel Testable and Diagnosable Phase-Frequency Detector. Circuits, Systems, and Signal Processing, 2014, 33, 999-1018. | 1.2 | 2 |
| 47 | Design and analysis of high linearity mixer using subharmonic technique. International Journal of Circuit Theory and Applications, 2018, 46, 2202-2216. | 1.3 | 2 |
| 48 | Selective counter design in quantum-dot cellular automata nanotechnology. Concurrency Computation Practice and Experience, 2022, 34, . | 1.4 | 2 |
| 49 | Systematic modeling and simulation of DLL-based frequency multiplier. , 2010, , . | | 1 |
| 50 | A DLL-based frequency synthesizer for VHF DVB-H/T receivers. , 2010, , . | | 1 |
| 51 | Covering VHF frequency band with novel DLL-based frequency synthesizer. , 2011, , . | | 1 |
| 52 | Design and analysis of negative capacitor by using MOSFETs. International Journal of Electronics, 2014, 101, 1167-1177. | 0.9 | 1 |
| 53 | A low power and jitter delay cell with pulse width modulation for wide range delay lock loops. Microelectronics Journal, 2021, 112, 105054. | 1.1 | 1 |
| 54 | Overview of Analog Wide Range Delay Locked Loops. Recent Advances in Electrical and Electronic Engineering, 2018, 11, 470-483. | 0.2 | 1 |