

Yu Cao

List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/941818/publications.pdf>

Version: 2024-02-01

272
papers

8,970
citations

71102

41
h-index

95266

68
g-index

282
all docs

282
docs citations

282
times ranked

6908
citing authors

#	ARTICLE	IF	CITATIONS
1	Energy harvesting efficiency analysis of counter-rotating horizontal-axis tidal turbines. Ships and Offshore Structures, 2022, 17, 1891-1900.	1.9	4
2	Impact of On-chip Interconnect on In-memory Acceleration of Deep Neural Networks. ACM Journal on Emerging Technologies in Computing Systems, 2022, 18, 1-22.	2.3	11
3	Optimization of interfacial characteristics of antimony sulfide selenide solar cells with double electron transport layer structure. Wuli Xuebao/Acta Physica Sinica, 2022, 71, 038802.	0.5	0
4	Origins of the Photocurrent Multiplication Effect in the Polythiophene-Based Photodetectors. Macromolecular Rapid Communications, 2022, , 2100928.	3.9	0
5	Efficient Sb ₂ S ₃ solar cells employing favorable (Sb ₄ S ₆) _n ribbon orientation via hydrothermal method. Materials Letters, 2022, 316, 132032.	2.6	10
6	Enhanced charge carrier transport via efficient grain conduction mode for Sb ₂ Se ₃ solar cell applications. Applied Surface Science, 2022, 591, 153169.	6.1	25
7	COIN: Communication-Aware In-Memory Acceleration for Graph Convolutional Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 472-485.	3.6	4
8	XST: A Crossbar Column-wise Sparse Training for Efficient Continual Learning. , 2022, , .		5
9	Epitaxial Growth of Vertically Aligned Antimony Selenide Nanorod Arrays for Heterostructure Based Self-Powered Photodetector. Advanced Optical Materials, 2022, 10, .	7.3	44
10	Safety analysis of an offshore platform for leakage and deflagration accidents from adjacent oil and gas storage and transportation units. Ships and Offshore Structures, 2021, 16, 815-826.	1.9	6
11	Bandgap grading of Sb ₂ (S,Se) ₃ for high-efficiency thin-film solar cells. Wuli Xuebao/Acta Physica Sinica, 2021, 70, 128802.	0.5	1
12	Theoretical Insight into High-Efficiency Triple-Junction Tandem Solar Cells via the Band Engineering of Antimony Chalcogenides. Solar Rrl, 2021, 5, 2000800.	5.8	70
13	SWIFT: Small-World-based Structural Pruning to Accelerate DNN Inference on FPGA. , 2021, , .		1
14	Robust RRAM-based In-Memory Computing in Light of Model Stability. , 2021, , .		12
15	Interconnect-Centric Benchmarking of In-Memory Acceleration for DNNS. , 2021, , .		4
16	A Reconstruction Method for Missing Data in Power System Measurement Based on LSGAN. Frontiers in Energy Research, 2021, 9, .	2.3	9
17	Substrate dependence on (Sb ₄ Se ₆) _n ribbon orientations of antimony selenide thin films: Morphology, carrier transport and photovoltaic performance. Journal of Alloys and Compounds, 2021, 862, 158703.	5.5	40
18	Evolutionary NAS in Light of Model Stability for Accurate Continual Learning. , 2021, , .		1

#	ARTICLE	IF	CITATIONS
19	SIAM: Chiplet-based Scalable In-Memory Acceleration with Mesh for Deep Neural Networks. Transactions on Embedded Computing Systems, 2021, 20, 1-24.	2.9	20
20	Experimental tests and CFD simulations of a horizontal wave flow turbine under the joint waves and currents. Ocean Engineering, 2021, 237, 109480.	4.3	10
21	End-to-End FPGA-based Object Detection Using Pipelined CNN and Non-Maximum Suppression. , 2021, , .		7
22	Algorithm-Hardware Co-Optimization for Energy-Efficient Drone Detection on Resource-Constrained FPGA. , 2021, , .		4
23	System-Level Benchmarking of Chiplet-based IMC Architectures for Deep Neural Network Acceleration. , 2021, , .		3
24	Power Performance Analysis of Digital Standard Cells for 28 nm Bulk CMOS at Cryogenic Temperature Using BSIM Models. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 193-200.	1.5	6
25	Alternate Model Growth and Pruning for Efficient Training of Recommendation Systems. , 2021, , .		1
26	Automatic Compilation of Diverse CNNs Onto High-Performance FPGA Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 424-437.	2.7	45
27	Performance Modeling for CNN Inference Accelerators on FPGA. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 843-856.	2.7	33
28	Rotational design of charge carrier transport layers for optimal antimony trisulfide solar cells and its integration in tandem devices. Solar Energy Materials and Solar Cells, 2020, 206, 110279.	6.2	88
29	Accurate Inference With Inaccurate RRAM Devices: A Joint Algorithm-Design Solution. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 27-35.	1.5	24
30	Noise-based Selection of Robust Inherited Model for Accurate Continual Learning. , 2020, , .		6
31	GAR: Graph Assisted Reasoning for Object Detection. , 2020, , .		12
32	Online Knowledge Acquisition with the Selective Inherited Model. , 2020, , .		1
33	Dual-function of CdCl ₂ treated SnO ₂ in Sb ₂ Se ₃ solar cells. Applied Surface Science, 2020, 534, 147632.	6.1	30
34	Accurate Inference with Inaccurate RRAM Devices: Statistical Data, Model Transfer, and On-line Adaptation. , 2020, , .		25
35	A Latency-Optimized Reconfigurable NoC for In-Memory Acceleration of DNNs. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 362-375.	3.6	25
36	A novel and fast method to prepare a Cu-supported $\text{In}_2\text{Sb}_2\text{S}_3$ @CuSbS ₂ binder-free electrode for sodium-ion batteries. RSC Advances, 2020, 10, 29567-29574.	3.6	15

#	ARTICLE	IF	CITATIONS
37	A Method for Cleaning Power Grid Operation Data Based on Spatiotemporal Correlation Constraints. IEEE Access, 2020, 8, 224741-224749.	4.2	5
38	Air-stable N-type printed carbon nanotube thin film transistors for CMOS logic circuits. Carbon, 2020, 163, 145-153.	10.3	31
39	Interconnect-Aware Area and Energy Optimization for In-Memory Acceleration of DNNs. IEEE Design and Test, 2020, 37, 79-87.	1.2	25
40	Ultrathin microcrystalline hydrogenated Si/Ge alloyed tandem solar cells towards full solar spectrum conversion. Frontiers of Chemical Science and Engineering, 2020, 14, 997-1005.	4.4	32
41	MNSIM 2.0: A Behavior-Level Modeling Tool for Memristor-based Neuromorphic Computing Systems. , 2020, , .		35
42	Interfacial Modification of Mesoporous TiO ₂ Films with PbI ₂ -Ethanolamine-Dimethyl Sulfoxide Solution for CsPbI ₃ Perovskite Solar Cells. Nanomaterials, 2020, 10, 962.	4.1	5
43	DAT-RNN: Trajectory Prediction with Diverse Attention. , 2020, , .		1
44	Efficient and Modularized Training on FPGA for Real-time Applications. , 2020, , .		1
45	Non-uniform DNN Structured Subnets Sampling for Dynamic Inference. , 2020, , .		8
46	FPGA-based low-batch training accelerator for modern CNNs featuring high bandwidth memory. , 2020, , .		17
47	Deep Neural Network Training Accelerator Designs in ASIC and FPGA. , 2020, , .		11
48	Small-world-based Structural Pruning for Efficient FPGA Inference of Deep Neural Networks. , 2020, , .		6
49	Formation mechanism of concentric and colorful ring perovskite films. Synthetic Metals, 2019, 255, 116107.	3.9	1
50	Towards Efficient Neural Networks On-A-Chip: Joint Hardware-Algorithm Approaches. , 2019, , .		6
51	Efficient Network Construction Through Structural Plasticity. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 453-464.	3.6	8
52	A Real-Time 17-Scale Object Detection Accelerator With Adaptive 2000-Stage Classification in 65 nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3843-3853.	5.4	5
53	Guest Editorsâ€™ Introduction to the Special Section on Hardware and Algorithms for Energy-Constrained On-chip Machine Learning. ACM Journal on Emerging Technologies in Computing Systems, 2019, 15, 1-2.	2.3	0
54	A 1.06- μ W Smart ECG Processor in 65-nm CMOS for Real-Time Biometric Authentication and Personal Cardiac Monitoring. IEEE Journal of Solid-State Circuits, 2019, 54, 2316-2326.	5.4	53

#	ARTICLE	IF	CITATIONS
55	Towards high efficiency inverted Sb ₂ Se ₃ thin film solar cells. Solar Energy Materials and Solar Cells, 2019, 200, 109945.	6.2	132
56	Single-Net Continual Learning with Progressive Segmented Training. , 2019, , .		7
57	Automatic Compiler Based FPGA Accelerator for CNN Training. , 2019, , .		31
58	Photochemical and Electrochemical Carbon Dioxide Utilization with Organic Compounds. Chinese Journal of Chemistry, 2018, 36, 644-659.	4.9	161
59	Process Scalability of Pulse-Based Circuits for Analog Image Convolution. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 2929-2938.	5.4	0
60	Optimizing the Convolution Operation to Accelerate Deep Neural Networks on FPGA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1354-1367.	3.1	225
61	Adaptive accelerated aging for 28 nm HKMG technology. Microelectronics Reliability, 2018, 80, 149-154.	1.7	3
62	ALAMO: FPGA acceleration of deep learning algorithms with a modularized RTL compiler. The Integration VLSI Journal, 2018, 62, 14-23.	2.1	68
63	Algorithm-hardware co-design of single shot detector for fast object detection on FPGAs. , 2018, , .		19
64	Large-Scale Neuromorphic Spiking Array Processors: A Quest to Mimic the Brain. Frontiers in Neuroscience, 2018, 12, 891.	2.8	177
65	Generative Sensing: Transforming Unreliable Sensor Data for Reliable Recognition. , 2018, , .		3
66	Power, Performance, and Area Benefit of Monolithic 3D ICs for On-Chip Deep Neural Networks Targeting Speech Recognition. ACM Journal on Emerging Technologies in Computing Systems, 2018, 14, 1-19.	2.3	3
67	Towards a Wearable Cough Detector Based on Neural Networks. , 2018, , .		13
68	Compact modeling and simulation of accelerated circuit aging. , 2018, , .		4
69	Inside Back Cover: Photochemical and Electrochemical Carbon Dioxide Utilization with Organic Compounds (Chin. J. Chem. 7/2018). Chinese Journal of Chemistry, 2018, 36, 671-671.	4.9	0
70	Integrative Photoreduction of CO ₂ with Subsequent Carbonylation: Photocatalysis for Reductive Functionalization of CO ₂ . ChemSusChem, 2018, 11, 3382-3387.	6.8	40
71	Accelerated BTI degradation under stochastic TDDB effect. , 2018, , .		3
72	Cost-Effective Design Solutions for Enhancing PRAM Reliability and Performance. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 1-11.	2.4	6

#	ARTICLE	IF	CITATIONS
73	A real-time 17-scale object detection accelerator with adaptive 2000-stage classification in 65nm CMOS. , 2017, , .		0
74	Optimizing Loop Operation and Dataflow in FPGA Acceleration of Deep Convolutional Neural Networks. , 2017, , .		244
75	Cathode Materials: Atomic Insights into the Enhanced Surface Stability in High Voltage Cathode Materials by Ultrathin Coating (Adv. Funct. Mater. 7/2017). Advanced Functional Materials, 2017, 27, .	14.9	0
76	RTN in Scaled Transistors for On-Chip Random Seed Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2248-2257.	3.1	17
77	Improving efficiency in sparse learning with the feedforward inhibitory motif. Neurocomputing, 2017, 267, 141-151.	5.9	3
78	Assessment of Self-Assembled Monolayers as High-Performance Thermal Interface Materials. Advanced Materials Interfaces, 2017, 4, 1700355.	3.7	16
79	TDDDB in HfSiON/SiO ₂ dielectric stack: Attiker probe based NEGF modeling, prediction and experiment. , 2017, , .		1
80	Atomic Insights into the Enhanced Surface Stability in High Voltage Cathode Materials by Ultrathin Coating. Advanced Functional Materials, 2017, 27, 1602873.	14.9	37
81	An automatic RTL compiler for high-throughput FPGA implementation of diverse deep convolutional neural networks. , 2017, , .		86
82	Review of Electronics Based on Single-Walled Carbon Nanotubes. Topics in Current Chemistry, 2017, 375, 75.	5.8	43
83	MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, , 1-1.	2.7	42
84	Adaptive accelerated aging with 28nm HKMG technology. , 2017, , .		2
85	Efficient prediction of 28nm path delay degradation under activity uncertainty. , 2017, , .		0
86	Optimizing Interfacial Cross-Linking in Graphene-Derived Materials, Which Balances Intralayer and Interlayer Load Transfer. ACS Applied Materials & Interfaces, 2017, 9, 24830-24839.	8.0	31
87	A 1.06 μ W smart ecg processor in 65 nm cmos for real-time biometric authentication and personal cardiac monitoring. , 2017, , .		7
88	Guest Editorial Special Issue on Nanoelectronic Devices and Circuits for Next Generation Sensing and Information Processing. IEEE Nanotechnology Magazine, 2017, 16, 383-386.	2.0	1
89	Algorithm and hardware design of discrete-time spiking neural networks based on back propagation with binary activations. , 2017, , .		39
90	Random sparse adaptation for accurate inference with inaccurate multi-level RRAM arrays. , 2017, , .		23

#	ARTICLE	IF	CITATIONS
91	End-to-end scalable FPGA accelerator for deep residual networks. , 2017, , .		39
92	A real-time 17-scale object detection accelerator with adaptive 2000-stage classification in 65nm CMOS. , 2017, , .		0
93	Monolithic 3D IC designs for low-power deep neural networks targeting speech recognition. , 2017, , .		6
94	Peripheral Circuit Design Considerations of Neuro-inspired Architectures. , 2017, , 167-182.		3
95	Bi-Level Rare Temporal Pattern Detection. , 2016, , .		9
96	High-performance radio frequency transistors based on diameter-separated semiconducting carbon nanotubes. Applied Physics Letters, 2016, 108, 233105.	3.3	18
97	Optimizing Latency, Energy, and Reliability of 1T1R ReRAM Through Cross-Layer Techniques. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 352-363.	3.6	15
98	Throughput-Optimized OpenCL-based FPGA Accelerator for Large-Scale Convolutional Neural Networks. , 2016, , .		379
99	Scalable and modularized RTL compilation of Convolutional Neural Networks onto FPGA. , 2016, , .		34
100	High-performance face detection with CPU-FPGA acceleration. , 2016, , .		8
101	Compact oscillation neuron exploiting metal-insulator-transition for neuromorphic computing. , 2016, , .		28
102	Design of a reliable RRAM-based PUF for compact hardware security primitives. , 2016, , .		5
103	Reducing the Model Order of Deep Neural Networks Using Information Theory. , 2016, , .		3
104	Hardware-efficient learning with feedforward inhibition. , 2016, , .		1
105	Carbon Nanotube Macroelectronics for Active Matrix Polymer-Dispersed Liquid Crystal Displays. ACS Nano, 2016, 10, 10068-10074.	14.6	44
106	Ranking the parameters of deep neural networks using the fisher information. , 2016, , .		7
107	Radio Frequency Transistors Using Aligned Semiconducting Carbon Nanotubes with Current-Gain Cutoff Frequency and Maximum Oscillation Frequency Simultaneously Greater than 70 GHz. ACS Nano, 2016, 10, 6782-6790.	14.6	63
108	A 65 nm Programmable ANalog Device Array (PANDA) for Analog Circuit Emulation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 181-190.	5.4	19

#	ARTICLE	IF	CITATIONS
109	Radio frequency transistors based on ultra-high purity semiconducting carbon nanotubes with superior extrinsic maximum oscillation frequency. Nano Research, 2016, 9, 363-371.	10.4	26
110	Imperceptible and Ultraflexible p-Type Transistors and Macroelectronics Based on Carbon Nanotubes. ACS Nano, 2016, 10, 199-206.	14.6	43
111	Non-uniform distribution in $\text{Si}_{1-x}\text{Ge}_x\text{H}$ and its influence on thin film and device performance. Solar Energy Materials and Solar Cells, 2016, 151, 1-6.	6.2	16
112	Bridged bis(β -cyclodextrin)s-based polysaccharide nanoparticles for controlled paclitaxel delivery. RSC Advances, 2016, 6, 28593-28598.	3.6	14
113	Technological Exploration of RRAM Crossbar Array for Matrix-Vector Multiplication. Journal of Computer Science and Technology, 2016, 31, 3-19.	1.5	117
114	Simulation, fabrication, and application of transparent conductive Mo-doped ZnO film in a solar cell. Solar Energy Materials and Solar Cells, 2016, 145, 171-179.	6.2	35
115	MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System. , 2016, , .		27
116	Mitigating effects of non-ideal synaptic device characteristics for on-chip learning. , 2015, , .		165
117	Scaling-up resistive synaptic arrays for neuro-inspired architecture: Challenges and prospect. , 2015, , .		128
118	Technology-design Co-optimization of Resistive Cross-point Array for Accelerating Learning Algorithms on Chip. , 2015, , .		50
119	Parallel Architecture With Resistive Crosspoint Array for Dictionary Learning Acceleration. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 194-204.	3.6	53
120	Technological exploration of RRAM crossbar array for matrix-vector multiplication. , 2015, , .		16
121	A Finite-Point Method for Efficient Gate Characterization Under Multiple Input Switching. ACM Transactions on Design Automation of Electronic Systems, 2015, 21, 1-25.	2.6	4
122	Duty cycle shift under static/dynamic aging in 28nm HK-MG technology. , 2015, , .		1
123	Energy-efficient reconstruction of compressively sensed bioelectrical signals with stochastic computing circuits. , 2015, , .		2
124	Programming strategies to improve energy efficiency and reliability of ReRAM memory systems. , 2015, , .		8
125	Fully parallel write/read in resistive synaptic array for accelerating on-chip learning. Nanotechnology, 2015, 26, 455204.	2.6	109
126	Optimizing latency, energy, and reliability of 1T1R ReRAM through appropriate voltage settings. , 2015, , .		16

#	ARTICLE	IF	CITATIONS
127	Band gap grading in microcrystalline silicon germanium thin film solar cells. Journal of Alloys and Compounds, 2015, 632, 456-459.	5.5	16
128	Finite-point method for efficient timing characterization of sequential elements. The Integration VLSI Journal, 2015, 49, 104-113.	2.1	0
129	On-chip Sparse Learning with Resistive Cross-point Array Architecture. , 2015, , .		4
130	Impact of temporal transistor variations on circuit reliability. , 2015, , .		3
131	On-Chip Sparse Learning Acceleration With CMOS and Resistive Synaptic Devices. IEEE Nanotechnology Magazine, 2015, 14, 969-979.	2.0	21
132	Accelerated Aging in Analog and Digital Circuits With Feedback. IEEE Transactions on Device and Materials Reliability, 2015, 15, 384-393.	2.0	19
133	Exploiting resistive cross-point array for compact design of physical unclonable function. , 2015, , .		38
134	Compact Modeling of BTI for Circuit Reliability Analysis. , 2015, , 93-119.		6
135	Novel voltage step stress (VSS) technique for fast lifetime prediction of hot carrier degradation. , 2014, , .		2
136	The Stochastic Loss of Spikes in Spiking Neural P Systems: Design and Implementation of Reliable Arithmetic Circuits. Fundamenta Informaticae, 2014, 134, 183-200.	0.4	11
137	Neurophysics-inspired parallel architecture with resistive crosspoint array for dictionary learning. , 2014, , .		11
138	BTI-Induced Aging under Random Stress Waveforms. , 2014, , .		12
139	Screen Printing as a Scalable and Low-Cost Approach for Rigid and Flexible Thin-Film Transistors Using Separated Carbon Nanotubes. ACS Nano, 2014, 8, 12769-12776.	14.6	179
140	Charge trapping in aligned single-walled carbon nanotube arrays induced by ionizing radiation exposure. Journal of Applied Physics, 2014, 115, 054506.	2.5	17
141	Statistical analysis of random telegraph noise in digital circuits. , 2014, , .		5
142	Low cost ECC schemes for improving the reliability of DRAM+PRAMMAIN memory systems. , 2014, , .		1
143	Parallel Programming of Resistive Cross-point Array for Synaptic Plasticity. Procedia Computer Science, 2014, 41, 126-133.	2.0	13
144	A Low Cost Multi-Tiered Approach to Improving the Reliability of Multi-Level Cell Pram. Journal of Signal Processing Systems, 2014, 76, 133-147.	2.1	5

#	ARTICLE	IF	CITATIONS
145	GaAs Nanowire Array Solar Cells with Axial p-n Junctions. Nano Letters, 2014, 14, 3293-3303.	9.1	168
146	p-Sulfonatocalix[4]arene-induced amphiphilic aggregation of fluorocarbon surfactant. Science China Chemistry, 2014, 57, 371-378.	8.2	13
147	Where is the Achilles Heel under Circuit Aging. , 2014, , .		1
148	Diagnosing bias runaway in analog/mixed signal circuits. , 2014, , .		8
149	Compact modeling of STT-MTJ devices. Solid-State Electronics, 2014, 102, 76-81.	1.4	19
150	Cross-Layer Modeling and Simulation of Circuit Reliability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 8-23.	2.7	48
151	Optical absorption enhancement of $\frac{1}{4}$ c-SiGe:H films deposited via high pressure and high power. Optoelectronics Letters, 2014, 10, 202-205.	0.8	7
152	Large-scale complementary macroelectronics using hybrid integration of carbon nanotubes and IGZO thin-film transistors. Nature Communications, 2014, 5, 4097.	12.8	233
153	BTI-induced aging under random stress waveforms: Modeling, simulation and silicon validation. , 2014, , .		1
154	Multilevel Reliability Simulation for IC Design. , 2014, , 719-749.		2
155	Charge Trapping in MOSFETS: BTI and RTN Modeling for Circuits. , 2014, , 751-782.		2
156	Effects of seed layer on the performance of microcrystalline silicon germanium solar cells. Journal of Semiconductors, 2013, 34, 034008.	3.7	2
157	Hydrogenated microcrystalline silicon germanium as bottom sub-cell absorber for triple junction solar cell. Solar Energy Materials and Solar Cells, 2013, 114, 161-164.	6.2	19
158	ACE: A robust variability and aging sensor for high-k/metal gate SoC. , 2013, , .		1
159	Logarithmic modeling of BTI under dynamic circuit operation: Static, dynamic and long-term prediction. , 2013, , .		11
160	Compact Modeling of Statistical BTI Under Trapping/Detrapping. IEEE Transactions on Electron Devices, 2013, 60, 3645-3654.	3.0	67
161	Compact modeling of STT-MTJ for SPICE simulation. , 2013, , .		6
162	Failure Analysis of Asymmetric Aging Under NBTI. IEEE Transactions on Device and Materials Reliability, 2013, 13, 340-349.	2.0	17

#	ARTICLE	IF	CITATIONS
163	Phosphatase-responsive amphiphilic calixarene assembly. RSC Advances, 2013, 3, 8058.	3.6	42
164	Numerical study on effects of random dopant fluctuation in double gate tunneling FET. , 2013, , .		2
165	Programmable ANalog Device Array (PANDA): A Methodology for Transistor-Level Analog Emulation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 1369-1380.	5.4	6
166	NBTI-aware circuit node criticality computation. ACM Journal on Emerging Technologies in Computing Systems, 2013, 9, 1-19.	2.3	9
167	A self-tuning design methodology for power-efficient multi-core systems. ACM Transactions on Design Automation of Electronic Systems, 2013, 18, 1-24.	2.6	7
168	Numerical simulation of a triple-junction thin-film solar cell based on $\frac{1}{4}\text{c-Si}_{1-x}\text{i}_{x/\text{sub}}\text{Ge}_{x/\text{sub}}\text{H}$. Chinese Physics B, 2013, 22, 098803.	1.4	5
169	Evaluation and mitigation of performance degradation under random telegraph noise for digital circuits. IET Circuits, Devices and Systems, 2013, 7, 273-282.	1.4	0
170	Logarithm Cofactor Difference Extrema Method of MOSFET's Post-Breakdown Current and Application to Parameter Extraction. Journal of Computational and Theoretical Nanoscience, 2013, 10, 669-672.	0.4	0
171	Numerical Electron Mobility Model of Nanoscale Symmetric, Asymmetric and Independent Double-Gate MOSFETs. Journal of Computational and Theoretical Nanoscience, 2013, 10, 763-771.	0.4	0
172	Aging statistics based on trapping/detrapping: Silicon evidence, modeling and long-term prediction. , 2012, , .		31
173	Hierarchical modeling of Phase Change memory for reliable design. , 2012, , .		14
174	Exploring sub-20nm FinFET design with predictive technology models. , 2012, , .		220
175	Asymmetric Aging and Workload Sensitive Bias Temperature Instability Sensors. IEEE Design and Test of Computers, 2012, 29, 18-26.	1.0	16
176	Physics matters. , 2012, , .		42
177	Statistical aging under dynamic voltage scaling: A logarithmic model approach. , 2012, , .		12
178	Multi-Tiered Approach to Improving the Reliability of Multi-Level Cell PRAM. , 2012, , .		2
179	Temporal Performance Degradation under RTN: Evaluation and Mitigation for Nanoscale Circuits. , 2012, , .		7
180	An analytical approach to efficient circuit variability analysis in scaled CMOS design. , 2012, , .		15

#	ARTICLE	IF	CITATIONS
181	Variation-Aware Supply Voltage Assignment for Simultaneous Power and Aging Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2143-2147.	3.1	23
182	Design benchmarking to 7nm with FinFET predictive technology models. , 2012, , .		26
183	Improving reliability of non-volatile memory technologies through circuit level techniques and error control coding. Eurasip Journal on Advances in Signal Processing, 2012, 2012, .	1.7	18
184	Enhancing the Reliability of STT-RAM through Circuit and System Level Techniques. , 2012, , .		32
185	Multi-level reliability simulation for IC design. , 2012, , .		0
186	The potential of Fe-FET for robust design under variations: A compact modeling study. Microelectronics Journal, 2012, 43, 898-903.	2.0	6
187	Effect of Electrolyte and Temperature on Interfacial Tensions of Alkylbenzene Sulfonate Solutions. Energy & Fuels, 2012, 26, 2175-2181.	5.1	78
188	Active roles of helium in the growth of hydrogenated microcrystalline silicon germanium thin films. Thin Solid Films, 2012, 520, 5940-5945.	1.8	11
189	A workload-aware neuromorphic controller for dynamic power and thermal management. , 2011, , .		0
190	Failure diagnosis of asymmetric aging under NBTI. , 2011, , .		18
191	Circuit-level delay modeling considering both TDDDB and NBTI. , 2011, , .		13
192	Intrinsic Variability and Reliability in Nano-CMOS. ECS Transactions, 2011, 35, 353-367.	0.5	1
193	A TDC-based test platform for dynamic circuit aging characterization. , 2011, , .		17
194	Predictive Modeling of Carbon Nanotube Devices. Integrated Circuits and Systems, 2011, , 141-164.	0.2	0
195	Correlation of no trouble found errors to Negative Bias Temperature Instability. , 2011, , .		0
196	Leakage Power and Circuit Aging Cooptimization by Gate Replacement Techniques. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 615-628.	3.1	49
197	Statistical Modeling and Simulation of Threshold Variation Under Random Dopant Fluctuations and Line-Edge Roughness. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 987-996.	3.1	62
198	Workload-Aware Neuromorphic Design of the Power Controller. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 381-390.	3.6	8

#	ARTICLE	IF	CITATIONS
199	Self-Tuning for Maximized Lifetime Energy-Efficiency in the Presence of Circuit Aging. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 760-773.	2.7	79
200	Low temperature deposition of high open-circuit voltage (>1.0V) n type amorphous silicon solar cells. Solar Energy Materials and Solar Cells, 2011, 95, 1922-1926.	6.2	24
201	Design sensitivity of single event transients in scaled logic circuits. , 2011, , .		14
202	Performance Enhancement of On-Chip Inductors With Permalloy Magnetic Rings. IEEE Electron Device Letters, 2011, 32, 69-71.	3.9	46
203	The impact of correlation between NBTI and TDDDB on the performance of digital circuits. , 2011, , .		5
204	Open-circuit voltage analysis of n type amorphous silicon solar cells deposited at low temperature. Chinese Physics B, 2011, 20, 087309.	1.4	6
205	Sub-100 nm scale on-chip inductors with CoZrTa for GHz applications. Journal of Applied Physics, 2011, 109, .	2.5	20
206	Programmable analog device array (PANDA). , 2011, , .		9
207	Modeling of Interconnect Parasitics. Integrated Circuits and Systems, 2011, , 81-103.	0.2	3
208	In-situ characterization and extraction of SRAM variability. , 2010, , .		3
209	Random variability modeling and its impact on scaled CMOS circuits. Journal of Computational Electronics, 2010, 9, 108-113.	2.5	55
210	Tuning the permeability of permalloy films for on-chip inductor applications. Applied Physics Letters, 2010, 97, 162506.	3.3	61
211	On the bias dependence of time exponent in NBTI and CHC effects. , 2010, , .		6
212	A self-evolving design methodology for power efficient multi-core systems. , 2010, , .		3
213	Compact modeling of Fe-FET and implications on variation-insensitive design. , 2010, , .		7
214	A resilience roadmap. , 2010, , .		73
215	Intrinsic variability in nano-CMOS design and beyond. , 2010, , .		0
216	Workload-adaptive process tuning strategy for power-efficient multi-core processors. , 2010, , .		3

#	ARTICLE	IF	CITATIONS
217	Workload-aware neuromorphic design of low-power supply voltage controller. , 2010, , .		2
218	Guest Editors' Introduction: Compact Variability Modeling in Scaled CMOS Design. IEEE Design and Test of Computers, 2010, 27, 6-7.	1.0	0
219	Modeling and Analysis of the Nonrectangular Gate Effect for Postlithography Circuit Simulation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 666-670.	3.1	1
220	Simulation of random telegraph Noise with 2-stage equivalent circuit. , 2010, , .		14
221	Optimized self-tuning for circuit aging. , 2010, , .		19
222	The Impact of NBTI Effect on Combinational Circuit: Modeling, Simulation, and Analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 173-183.	3.1	243
223	Improved Frequency Response of On-Chip Inductors With Patterned Magnetic Dots. IEEE Electron Device Letters, 2010, 31, 207-209.	3.9	28
224	Pathfinding for 22nm CMOS designs using Predictive Technology Models. , 2009, , .		9
225	Variation-aware supply voltage assignment for minimizing circuit degradation and leakage. , 2009, , .		11
226	Field-Based Capacitance Modeling for Sub-65-nm On-Chip Interconnect. IEEE Transactions on Electron Devices, 2009, 56, 1862-1872.	3.0	45
227	Compact Model of Carbon Nanotube Transistor and Interconnect. IEEE Transactions on Electron Devices, 2009, 56, 2232-2242.	3.0	21
228	New-Age: A Negative Bias Temperature Instability-Estimation Framework for Microarchitectural Components. International Journal of Parallel Programming, 2009, 37, 417-431.	1.5	11
229	Compact modeling of a PD SOI MESFET for wide temperature designs. Microelectronics Journal, 2009, 40, 1264-1273.	2.0	9
230	On the efficacy of input Vector Control to mitigate NBTI effects and leakage power. , 2009, , .		56
231	Guest Editors' Introduction: Reliability Challenges in Nano-CMOS Design. IEEE Design and Test of Computers, 2009, 26, 6-7.	1.0	22
232	Enabling resonant clock distribution with scaled on-chip magnetic inductors. , 2009, , .		1
233	Compact Modeling of Stress Effects in Scaled CMOS. , 2009, , .		6
234	Finite-Point-Based Transistor Model: A New Approach to Fast Circuit Simulation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1470-1480.	3.1	3

#	ARTICLE	IF	CITATIONS
235	Circuit aging prediction for low-power operation. , 2009, , .		36
236	Modeling and simulation of transistor performance shift under pattern-dependent RTA process. , 2009, , .		0
237	The Predictive Technology Model in the Late Silicon Era and Beyond. Foundations and Trends in Electronic Design Automation, 2009, 3, 305-401.	1.0	7
238	Digital Circuit Design Challenges and Opportunities in the Era of Nanoscale CMOS. Proceedings of the IEEE, 2008, 96, 343-365.	21.8	165
239	Reliable Systems on Unreliable Fabrics. IEEE Design and Test of Computers, 2008, 25, 322-332.	1.0	48
240	Projection-Based Piecewise-Linear Response Surface Modeling for Strongly Nonlinear VLSI Performance Variations. , 2008, , .		4
241	Statistical prediction of circuit aging under process variations. , 2008, , .		59
242	Design rule optimization of regular layout for leakage reduction in nanoscale design. , 2008, , .		8
243	Optimized Circuit Failure Prediction for Aging: Practicality and Promise. , 2008, , .		111
244	Statistical modeling and simulation of threshold variation under dopant fluctuations and line-edge roughness. , 2008, , .		46
245	Finite-Point Gate Model for Fast Timing and Power Analysis. , 2008, , .		2
246	The impact of NBTI on the performance of combinational and sequential circuits. Proceedings - Design Automation Conference, 2007, , .	0.0	121
247	Modeling and analysis of non-rectangular gate for post-lithography circuit simulation. Proceedings - Design Automation Conference, 2007, , .	0.0	25
248	Compact Modeling of a PD SOI MESFET for Wide Temperature Designs. , 2007, , .		1
249	Mapping Statistical Process Variations Toward Circuit Performance Variability: An Analytical Modeling Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1866-1873.	2.7	53
250	Predictive technology model for nano-CMOS design exploration. ACM Journal on Emerging Technologies in Computing Systems, 2007, 3, 1.	2.3	190
251	Predictive technology modeling for 32nm low power design. , 2007, , .		7
252	Compact modeling of carbon nanotube transistor for early stage process-design exploration. , 2007, , .		61

#	ARTICLE	IF	CITATIONS
253	An efficient method to identify critical gates under circuit aging. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	48
254	A robust finite-point based gate model considering process variations. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	6
255	Rigorous extraction of process variations for 65nm CMOS design. , 2007, , .		12
256	Rigorous extraction of process variations for 65nm CMOS design. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	4
257	An Integrated Modeling Paradigm of Circuit Reliability for 65nm CMOS Technology. , 2007, , .		14
258	A New Simulation Method for NBTI Analysis in SPICE Environment. , 2007, , .		12
259	Compact Modeling and Simulation of Circuit Reliability for 65-nm CMOS Technology. IEEE Transactions on Device and Materials Reliability, 2007, 7, 509-517.	2.0	267
260	The Impact of NBTI on the Performance of Combinational and Sequential Circuits. Proceedings - Design Automation Conference, 2007, , .	0.0	45
261	Modeling and minimization of PMOS NBTI effect for robust nanometer design. , 2006, , .		301
262	Predictive Modeling of the NBTI Effect for Reliable Design. , 2006, , .		321
263	Predictive Technology Model for Nano-CMOS Design Exploration. , 2006, , .		11
264	Modeling and minimization of PMOS NBTI effect for robust nanometer design. Proceedings - Design Automation Conference, 2006, , .	0.0	31
265	Mapping statistical process variations toward circuit performance variability. , 2005, , .		75
266	Switch-factor based loop RLC modeling for efficient timing analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 1072-1078.	3.1	8
267	Impact of on-chip interconnect frequency-dependent R(f)L(f) on digital and RF design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 158-162.	3.1	13
268	Robust design of high fan-in/out subthreshold circuits. , 0, , .		7
269	Statistical leakage minimization through joint selection of gate sizes, gate lengths and threshold voltage. , 0, , .		4
270	New Generation of Predictive Technology Model for Sub-45nm Design Exploration. , 0, , .		233

#	ARTICLE	IF	CITATIONS
271	LOTUS: Leakage Optimization under Timing Uncertainty for Standard-cell designs. , 0, , .		4
272	VLSI. , 0, , .		1