Xiao-Chun Ye

List of Publications by Year
in descending order

30 papers	376 citations	1478505 6 h-index	1125743 13 g-index
30 all docs	30 docs citations	30 times ranked	218 citing authors

#	Article	IF	Citations
1	Sampling Methods for Efficient Training of Graph Convolutional Networks: A Survey. IEEE/CAA Journal of Automatica Sinica, 2022, 9, 205-234.	13.1	34
2	Accelerating Graph Processing With Lightweight Learning-Based Data Reordering. IEEE Computer Architecture Letters, 2022, 21, 5-8.	1.5	2
3	Characterizing and Understanding Distributed GNN Training on GPUs. IEEE Computer Architecture Letters, 2022, 21, 21-24.	1.5	3
4	LRP: Predictive output activation based on SVD approach for CNN s acceleration. , 2022, , .		4
5	Scalable and efficient graph traversal on high-throughput cluster. CCF Transactions on High Performance Computing, 2021, 3, 101-113.	1.7	0
6	Hardware Acceleration for GCNs via Bidirectional Fusion. IEEE Computer Architecture Letters, 2021, 20, 66-4.	1.5	3
7	Bit-Slice Butterfly Processing Units for 64-Point RSFQ FFT Processors. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-6.	1.7	5
8	A Reliability-Aware Joint Design Method of Application Mapping and Wavelength Assignment for WDM-Based Silicon Photonic Interconnects on Chip. IEEE Access, 2020, 8, 73457-73474.	4.2	4
9	Distributed Self-Clock: A Suitable Architecture for SFQ Circuits. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-7.	1.7	1
10	Design of an 8-bit Bit-Parallel RSFQ Microprocessor. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-6.	1.7	3
11	Characterizing and Understanding GCNs on GPU. IEEE Computer Architecture Letters, 2020, 19, 22-25.	1.5	35
12	HyGCN: A GCN Accelerator with Hybrid Architecture. , 2020, , .		160
13	Highly Efficient and GPU-Friendly Implementation of BFS on Single-node System. , 2020, , .		1
14	Pixel-Semantic Revising of Position: One-Stage Object Detector with Shared Encoder-Decoder. Communications in Computer and Information Science, 2020, , 516-525.	0.5	1
15	Logic Design of an 8-bit RSFQ Microprocessor. , 2019, , .		1
16	An 8-bit Bit-Slice TEA-Cryptographic Accelerator for 64-bit RSFQ Secure Coprocessors. , 2019, , .		2
17	C-MIDN: Coupled Multiple Instance Detection Network With Segmentation Guidance for Weakly Supervised Object Detection. , 2019, , .		26
18	Logic Design of a 16-bit Bit-Slice Shifter for 64-bit RSFQ Microprocessors. , 2019, , .		1

#	Article	IF	Citations
19	Design of Datapath Circuits for a Bit-Parallel 8-bit RSFQ Microprocessor. , 2019, , .		2
20	Applying CNN on a scientific application accelerator based on dataflow architecture. CCF Transactions on High Performance Computing, 2019, 1, 177-195.	1.7	2
21	A Non-Stop Double Buffering Mechanism for Dataflow Architecture. Journal of Computer Science and Technology, 2018, 33, 145-157.	1.5	10
22	A Pipelining Loop Optimization Method for Dataflow Architecture. Journal of Computer Science and Technology, 2018, 33, 116-130.	1.5	8
23	Logic Design of a 16-bit Bit-Slice Arithmetic Logic Unit for 32-/64-bit RSFQ Microprocessors. IEEE Transactions on Applied Superconductivity, 2018, 28, 1-5.	1.7	24
24	Optimizing network efficiency of dataflow architectures through dynamic packet merging. , 2018, , .		1
25	32-Bit 4 Ã— 4 Bit-Slice RSFQ Matrix Multiplier. IEEE Transactions on Applied Superconductivity, 2018, 28, 1-5.	1.7	5
26	An Efficient Network-on-Chip Router for Dataflow Architecture. Journal of Computer Science and Technology, 2017, 32, 11-25.	1.5	15
27	Memory partition for SIMD in streaming dataflow architectures. , 2016, , .		2
28	Low Execution Efficiency: When General Multi-core Processor Meets Wireless Communication Protocol. , 2013, , .		1
29	SimICT: A fast and flexible framework for performance and power evaluation of large-scale architecture. , 2013, , .		17
30	Auto-Tuning GEMV on Many-Core GPU. , 2012, , .		3