

Xiao-Chun Ye

List of Publications by Year in descending order

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Version: 2024-02-01

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papers

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1478505

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218
citing authors

| # | ARTICLE | IF | CITATIONS |
|----|---|------|-----------|
| 1 | HyGCN: A GCN Accelerator with Hybrid Architecture. , 2020, , . | | 160 |
| 2 | Characterizing and Understanding GCNs on GPU. IEEE Computer Architecture Letters, 2020, 19, 22-25. | 1.5 | 35 |
| 3 | Sampling Methods for Efficient Training of Graph Convolutional Networks: A Survey. IEEE/CAA Journal of Automatica Sinica, 2022, 9, 205-234. | 13.1 | 34 |
| 4 | C-MIDN: Coupled Multiple Instance Detection Network With Segmentation Guidance for Weakly Supervised Object Detection. , 2019, , . | | 26 |
| 5 | Logic Design of a 16-bit Bit-Slice Arithmetic Logic Unit for 32-/64-bit RSFQ Microprocessors. IEEE Transactions on Applied Superconductivity, 2018, 28, 1-5. | 1.7 | 24 |
| 6 | SimICT: A fast and flexible framework for performance and power evaluation of large-scale architecture. , 2013, , . | | 17 |
| 7 | An Efficient Network-on-Chip Router for Dataflow Architecture. Journal of Computer Science and Technology, 2017, 32, 11-25. | 1.5 | 15 |
| 8 | A Non-Stop Double Buffering Mechanism for Dataflow Architecture. Journal of Computer Science and Technology, 2018, 33, 145-157. | 1.5 | 10 |
| 9 | A Pipelining Loop Optimization Method for Dataflow Architecture. Journal of Computer Science and Technology, 2018, 33, 116-130. | 1.5 | 8 |
| 10 | 32-Bit 4 \times 4 Bit-Slice RSFQ Matrix Multiplier. IEEE Transactions on Applied Superconductivity, 2018, 28, 1-5. | 1.7 | 5 |
| 11 | Bit-Slice Butterfly Processing Units for 64-Point RSFQ FFT Processors. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-6. | 1.7 | 5 |
| 12 | A Reliability-Aware Joint Design Method of Application Mapping and Wavelength Assignment for WDM-Based Silicon Photonic Interconnects on Chip. IEEE Access, 2020, 8, 73457-73474. | 4.2 | 4 |
| 13 | LRP: Predictive output activation based on SVD approach for CNN s acceleration. , 2022, , . | | 4 |
| 14 | Auto-Tuning GEMV on Many-Core GPU. , 2012, , . | | 3 |
| 15 | Design of an 8-bit Bit-Parallel RSFQ Microprocessor. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-6. | 1.7 | 3 |
| 16 | Hardware Acceleration for GCNs via Bidirectional Fusion. IEEE Computer Architecture Letters, 2021, 20, 66-4. | 1.5 | 3 |
| 17 | Characterizing and Understanding Distributed GNN Training on GPUs. IEEE Computer Architecture Letters, 2022, 21, 21-24. | 1.5 | 3 |
| 18 | Memory partition for SIMD in streaming dataflow architectures. , 2016, , . | | 2 |

| # | ARTICLE | IF | CITATIONS |
|----|--|-----|-----------|
| 19 | An 8-bit Bit-Slice TEA-Cryptographic Accelerator for 64-bit RSFQ Secure Coprocessors. , 2019, , . | | 2 |
| 20 | Design of Datapath Circuits for a Bit-Parallel 8-bit RSFQ Microprocessor. , 2019, , . | | 2 |
| 21 | Applying CNN on a scientific application accelerator based on dataflow architecture. CCF Transactions on High Performance Computing, 2019, 1, 177-195. | 1.7 | 2 |
| 22 | Accelerating Graph Processing With Lightweight Learning-Based Data Reordering. IEEE Computer Architecture Letters, 2022, 21, 5-8. | 1.5 | 2 |
| 23 | Low Execution Efficiency: When General Multi-core Processor Meets Wireless Communication Protocol. , 2013, , . | | 1 |
| 24 | Optimizing network efficiency of dataflow architectures through dynamic packet merging. , 2018, , . | | 1 |
| 25 | Logic Design of an 8-bit RSFQ Microprocessor. , 2019, , . | | 1 |
| 26 | Logic Design of a 16-bit Bit-Slice Shifter for 64-bit RSFQ Microprocessors. , 2019, , . | | 1 |
| 27 | Distributed Self-Clock: A Suitable Architecture for SFQ Circuits. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-7. | 1.7 | 1 |
| 28 | Highly Efficient and GPU-Friendly Implementation of BFS on Single-node System. , 2020, , . | | 1 |
| 29 | Pixel-Semantic Revising of Position: One-Stage Object Detector with Shared Encoder-Decoder. Communications in Computer and Information Science, 2020, , 516-525. | 0.5 | 1 |
| 30 | Scalable and efficient graph traversal on high-throughput cluster. CCF Transactions on High Performance Computing, 2021, 3, 101-113. | 1.7 | 0 |