Adoracion Rueda

List of Publications by Year
in descending order

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122 papers	1,575 citations	430874 18 h-index	395702 33 g-index
123 all docs	123 docs citations	123 times ranked	776 citing authors

#	Article	IF	Citations
1	Nonlinear switched capacitor 'neural' networks for optimization problems. IEEE Transactions on Circuits and Systems, 1990, 37, 384-398.	0.9	244
2	A tissue impedance measurement chip for myocardial ischemia detection. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 2620-2628.	0.1	85
3	Chaos from switched-capacitor circuits: Discrete maps. Proceedings of the IEEE, 1987, 75, 1090-1106.	21.3	71
4	A highly sensitive microsystem based on nanomechanical biosensors for genomics applications. Sensors and Actuators B: Chemical, 2006, 118, 2-10.	7.8	68
5	Practical oscillation-based test of integrated filters. IEEE Design and Test of Computers, 2002, 19, 64-72.	1.0	67
6	A 1.25-V Micropower>tex<G_m>/tex<->tex<C>/tex<Filter Based on FGMOS Transistors Operating in Weak Inversion. IEEE Journal of Solid-State Circuits, 2004, 39, 100-111.	5.4	62
7	Testing mixed-signal cores: a practical oscillation-based test in an analog macrocell. IEEE Design and Test of Computers, 2002, 19, 73-82.	1.0	57
8	Testable switched-capacitor filters. IEEE Journal of Solid-State Circuits, 1993, 28, 719-724.	5.4	52
9	Low-power CMOS threshold-logic gate. Electronics Letters, 1995, 31, 2157-2159.	1.0	44
10	A 1-V Micropower Log-Domain Integrator Based on FGMOS Transistors Operating in Weak Inversion. IEEE Journal of Solid-State Circuits, 2004, 39, 256-259.	5.4	38
11	A practical floating-gate Muller-C element using vMOS threshold gates. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2001, 48, 102-106.	2.2	32
12	Alternate Test of LNAs Through Ensemble Learning of On-Chip Digital Envelope Signatures. Journal of Electronic Testing: Theory and Applications (JETTA), 2011, 27, 277-288.	1.2	29
13	On-chip sinusoidal signal generation with harmonic cancelation for analog and mixed-signal BIST applications. Analog Integrated Circuits and Signal Processing, 2015, 82, 67-79.	1.4	28
14	Impact of Random Channel Mismatch on the SNR and SFDR of Time-Interleaved ADCs. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 140-150.	0.1	25
15	The Bio-Oscillator: A Circuit for Cell-Culture Assays. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 164-168.	3.0	23
16	Background Digital Calibration of Comparator Offsets in Pipeline ADCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1345-1349.	3.1	23
17	Design of a CMOS closed-loop system with applications to bio-impedance measurements. Microelectronics Journal, 2010, 41, 231-239.	2.0	22
18	Oscillation-based test in bandpass oversampled A/D converters. Microelectronics Journal, 2003, 34, 927-936.	2.0	21

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19	Wave analogue filters using switched-current techniques. Electronics Letters, 1991, 27, 1482.	1.0	20
20	A high-Q bandpass fully differential SC filter with enhanced testability. IEEE Journal of Solid-State Circuits, 1998, 33, 976-986.	5.4	20
21	On-Chip Evaluation of Oscillation-Based-Test Output Signals for Switched-Capacitor Circuits. Analog Integrated Circuits and Signal Processing, 2002, 33, 201-211.	1.4	20
22	Nonlinear switched-capacitor networks: Basic principles and piecewise-linear design. IEEE Transactions on Circuits and Systems, 1985, 32, 305-319.	0.9	19
23	Programmable switched-current wave analog filters. IEEE Journal of Solid-State Circuits, 1994, 29, 927-935.	5.4	19
24	Oscillation-based test in oversampled Î£Î” modulators. Microelectronics Journal, 2002, 33, 799-806.	2.0	19
25	A method for bioimpedance measure with four- and two-electrode sensor systems. , 2008, 2008, 2318-21.		17
26	An integrated circuit for tissue impedance measure. , 0, , .		16
27	Low-Cost Digital Detection of Parametric Faults in Cascaded $SigmaDelta$ Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1326-1338.	5.4	16
28	Practical DfT strategy for fault diagnosis in active analogue filters. Electronics Letters, 1995, 31, 1221-1222.	1.0	15
29	Blind Adaptive Estimation of Integral Nonlinear Errors in ADCs Using Arbitrary Input Stimulus. IEEE Transactions on Instrumentation and Measurement, 2011, 60, 452-461.	4.7	15
30	Black-Box Calibration for ADCs With Hard Nonlinear Errors Using a Novel INL-Based Additive Code: A Pipeline ADC Case Study. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1718-1729.	5.4	15
31	Sine-Wave Signal Characterization Using Square-Wave and ??-Modulation: Application to Mixed-Signal BIST. Journal of Electronic Testing: Theory and Applications (JETTA), 2005, 21, 221-232.	1.2	14
32	2.4-GHz single-ended input low-power low-voltage active front-end for ZigBee applications in 90 nm CMOS. , 2011, , .		14
33	Improving the testability of switched-capacitor filters. Analog Integrated Circuits and Signal Processing, 1993, 4, 199-213.	1.4	13
34	Studying the effects of mismatching and clock-feedthrough in switched-current filters using behavioral simulation. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1997, 44, 1058-1067.	2.2	13
35	On-Chip Analog Sinewave Generator with Reduced Circuitry Resources. Midwest Symposium on Circuits and Systems, 2006, , .	1.0	12
36	On Chopper Effects in Discrete-Time $SigmaDelta$ Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2438-2449.	5.4	11

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37	Improving the Accuracy of RF Alternate Test Using Multi-VDD Conditions: Application to Envelope-Based Test of LNAs. , 2011, , .		11
38	Analog Sinewave Signal Generators for Mixed-Signal Built-in Test Applications. Journal of Electronic Testing: Theory and Applications (JETTA), 2011, 27, 305-320.	1.2	10
39	Synthesis of resistive n-port section-wise piecewise-linear networks. IEEE Transactions on Circuits and Systems, 1982, 29, 6-14.	0.9	9
40	Hazard-free edge-triggered D flipflop based on threshold gates. Electronics Letters, 1994, 30, 1390-1391.	1.0	9
41	A mixed-signal design reuse methodology based on parametric behavioural models with non-ideal effects. , 0, , .		9
42	Cascade modulator with digital correction for finite amplifier gain effects. Electronics Letters, 2004, 40, 1322.	1.0	9
43	On-chip characterisation of RF systems based on envelope response analysis. Electronics Letters, 2010, 46, 36.	1.0	9
44	INL systematic reduced-test technique for Pipeline ADCs. , 2014, , .		9
45	Canonical nonâ€linear programming circuits. International Journal of Circuit Theory and Applications, 1987, 15, 71-77.	2.0	8
46	A Simple and Secure Start-Up Circuitry for Oscillation-Based-Test Application. Analog Integrated Circuits and Signal Processing, 2002, 32, 187-190.	1.4	8
47	Enhanced double-histogram test. Electronics Letters, 2009, 45, 349.	1.0	8
48	A CMOS bio-impedance measurement system. , 2009, , .		8
49	Design trade-offs for on-chip driving of high-speed high-performance ADCs in static BIST applications. , 2016, , .		8
50	Chaos via a piecewise-linear switched-capacitor circuit. Electronics Letters, 1987, 23, 662.	1.0	7
51	Digital test for the extraction of integrator leakage in first- and second-order modulators. IET Circuits, Devices and Systems, 2004, 151, 349.	0.6	7
52	A 1.2V 5.14mW quadrature frequency synthesizer in 90nm CMOS technology for 2.4GHz ZigBee applications. , 2008, , .		7
53	Sinusoidal signal generation for mixed-signal BIST using a harmonic-cancellation technique. , 2013, , .		7
54	Sectionwise piecewise polynomial functions: Applications to the analysis and synthesis of nonlinear n- port networks. IEEE Transactions on Circuits and Systems, 1984, 31, 897-906.	0.9	6

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55	Practical oscillation-based test in analog integrated filters: experimental results. , 0, , .		6
56	A survey on digital background calibration of ADCs. , 2009, , .		6
57	Low-cost signature test of RF blocks based on envelope response analysis. , 2010, , .		6
58	Testability in analogue cellular neural networks. International Journal of Circuit Theory and Applications, 1992, 20, 583-587.	2.0	5
59	New BIST Schemes for Structural Testing of Pipelined Analog to Digital Converters. Journal of Electronic Testing: Theory and Applications (JETTA), 2001, 17, 373-383.	1.2	5
60	VHDL behavioural modelling of pipeline analog to digital converters. Measurement: Journal of the International Measurement Confederation, 2002, 31, 47-60.	5.0	5
61	Full Calibration Digital Techniques for Pipeline ADCs. , 0, , .		5
62	A CMOS optical PSD with submicrometer resolution. Analog Integrated Circuits and Signal Processing, 2007, 53, 109-118.	1.4	5
63	A BIST Solution for Frequency Domain Characterization of Analog Circuits. Journal of Electronic Testing: Theory and Applications (JETTA), 2010, 26, 429-441.	1.2	5
64	(Some) Open Problems to Incorporate BIST in Complex Heterogeneous Integrated Systems. , 2010, , .		5
65	A 3.6mW @ 1.2V high linear 8th-order CMOS complex filter for IEEE 802.15.4 standard. , 2011, , .		5
66	Linearity test of high-speed high-performance ADCs using a self-testable on-chip generator. , 2016, , .		5
67	Noisy signal based background technique for gain error correction in pipeline ADCs. IEE Proceedings: Computers and Digital Techniques, 2005, 152, 53.	1.6	4
68	A Sinewave Analyzer for Mixed-Signal BIST Applications in a 0.35 um Technology. , 2006, , .		4
69	Improved Background Algorithms for Pipeline ADC Full Calibration. , 2007, , .		4
70	A 5GHz wide tuning range LC-VCO in sub-micrometer CMOS technology. , 2008, , .		4
71	A BIST Solution for the Functional Characterization of RF Systems Based on Envelope Response Analysis. , 2009, , .		4
72	Fast adaptive comparator offset calibration in pipeline ADC with selfâ€repairing thermometer to binary encoder. International Journal of Circuit Theory and Applications, 2019, 47, 333-349.	2.0	4

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73	Practical solutions for the application of the oscillation-based-test: start-up and on-chip evaluation. , 0, , .		3
74	A low power low voltage mixer for 2.4GHz applications in CMOS-90nm technology. , 2010, , .		3
75	Guidelines for the efficient design of sinewave generators for analog/mixed-signal BIST. , 2010, , .		3
76	Closed-loop simulation method for evaluation of static offset in discrete-time comparators. , 2014, , .		3
77	Towards Bio-impedance Based Labs: A Review. J of Electrical Engineering, 2016, 4, .	0.1	3
78	Î½MOS-based Sorter for Arithmetic Applications. VLSI Design, 2000, 11, 129-136.	0.5	2
79	A continuous-time incremental analog to digital converter. , 0, , .		2
80	A charge correction cell for FGMOS-based circuits. , 0, , .		2
81	Digital background calibration technique for pipeline ADCs with multi-bit stages. , 0, , .		2
82	LP-LV high-performance monolithic DTMF receiver with on-chip test facilities. , 2003, , .		2
83	Behavioral Modeling of Multistage ADCS and Its Use for Design, Calibration and Test. , 2004, , 163-214.		2
84	Novel swapping technique for background calibration of capacitor mismatching in pipeline ADCS. , 2007, , .		2
85	New swapping technique for background calibration of capacitor mismatch and amplifier finite DC-gain in pipeline ADCs. Analog Integrated Circuits and Signal Processing, 2008, 57, 57-68.	1.4	2
86	A 2.4GHz LNA in a 90-nm CMOS technology designed with ACM model. , 2008, , .		2
87	Practical implementation of a network analyzer for analog BIST applications. , 2008, , .		2
88	Efficient functional built-in test for RF systems using two-tone response envelope analysis. , 2009, , .		2
89	Design of A CMOS closed-loop system useful for bio-impedance measurements. , 2009, , .		2
90	Oscillation-Based Test applied to cell culture monitoring. , 2013, , .		2

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91	A compact R-2R DAC for BIST applications. , 2016, , .		2
92	Static global models for linear nâ€port networks realized with operational amplifiers. International Journal of Circuit Theory and Applications, 1985, 13, 99-122.	2.0	1
93	Analog/mixed-signal IP modeling for design reuse. , 0, , .		1
94	A Low-Voltage Floating-Gate MOS Biquad. VLSI Design, 2001, 12, 407-414.	0.5	1
95	Threshold-logic-based design of compressors. , 0, , .		1
96	A Switched Opamp-Based Bandpass Filter: Design and Implementation in a 0.35 Î¼m CMOS Technology. Analog Integrated Circuits and Signal Processing, 2003, 34, 201-209.	1.4	1
97	Practical Implementation of a Network Analyzer for Analog BIST Applications. , 2008, , .		1
98	Practical test cores for the on-chip generation and evaluation of analog test signals: Application to a network/spectrum analyzer for analog BIST. , 2009, , .		1
99	On-line estimation of the integral non-linear errors in analogue-to-digital converters without histogram evaluation. , 2009, , .		1
100	An adaptive BIST for INL estimation of ADCs without histogram evaluation. , 2010, , .		1
101	On-chip biased voltage-controlled oscillator with temperature compensation of the oscillation amplitude for robust I/Q generation. , 2010, , .		1
102	Inductor characterization in RF LC-VCOs. , 2013, , .		1
103	Analysis of process variations' impact on a 2.4 GHz 90 nm CMOS LNA. , 2013, , .		1
104	Towards Bio-Impedance based labs: A review. , 2015, , .		1
105	Low-jitter differential clock driver circuits for high-performance high-resolution ADCs. , 2015, , .		1
106	Design methodology for low-jitter differential clock recovery circuits in high performance ADCs. Analog Integrated Circuits and Signal Processing, 2016, 89, 593-609.	1.4	1
107	Cell-culture measurements using voltage oscillations. , 2016, , .		1
108	An Application of Self-Timed Circuits to the Reduction of Switching Noise in Analog-Digital Circuits. Lecture Notes in Computer Science, 2000, , 295-305.	1.3	1

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109	New analogue switch circuit having very low forward resistance. Electronics Letters, 1984, 20, 488.	1.0	0
110	A novel all-capacitor MOS-compatible analogue multiplier. International Journal of Electronics, 1984, 57, 775-779.	1.4	0
111	New design technique for multiport regionalizers. International Journal of Electronics, 1985, 58, 445-454.	1.4	0
112	Low-cost BSA technique for threshold-logic gate based multiplier implementations. Electronics Letters, 1997, 33, 1028.	1.0	0
113	Testing mixed-signal cores. , 0, , .		0
114	vMOS-based compressor designs. , 0, , .		0
115	Low-Voltage CMOS Log-Companding Techniques for Audio Applications. Analog Integrated Circuits and Signal Processing, 2004, 38, 121-135.	1.4	0
116	Mixed-mode simulation of optical-based systems: PSD application. , 2005, 5839, 172.		0
117	Analysis of steady-state common-mode response in differential LC-VCOs. , 2012, , .		0
118	Self-biased input common-mode generation for improving dynamic range and yield in inverter-based filters. , 2012, , .		0
119	From voltage oscillations to tissue-impedance measurements. , 2015, , .		0
120	An approach to the design of low-jitter differential clock recovery circuits for high performance ADCs. , 2015, , .		0
121	Monitoring tissue evolution on electrodes with bio-impedance test. , 2016, , .		0
122	Test of Sigma-Delta converters. , 2008, , 235-276.		0