Elena Gnani

List of Publications by Year
in descending order

201	2,823	201658	223791
papers	citations	27 h-index	46 g-index

202	202	202	1915
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Characterization and numerical analysis of breakdown in thick amorphous SiO2 capacitors. Solid-State Electronics, 2022, 192, 108256.	1.4	1
2	On the breakdown voltage temperature dependence of high-voltage power diodes passivated with diamond-like carbon. Solid-State Electronics, 2022, 193, 108284.	1.4	2
3	Group velocity of electrons in 4H-SiC from Density Functional Theory simulations. Solid-State Electronics, 2022, 194, 108338.	1.4	2
4	Thickness-dependent dielectric breakdown in thick amorphous SiO2 capacitors. Solid-State Electronics, 2022, 194, 108363.	1.4	2
5	TCAD Investigation of Differently Doped DLC Passivation for Large-Area High-Power Diodes. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2021, 9, 2155-2162.	5.4	3
6	Novel TCAD Approach for the Investigation of Charge Transport in Thick Amorphous SiO₂ Insulators. IEEE Transactions on Electron Devices, 2021, 68, 5438-5447.	3.0	4
7	Influence of the DLC Passivation Conductivity on the Performance of Silicon High-Power Diodes Over an Extended Temperature Range. IEEE Journal of the Electron Devices Society, 2021, 9, 431-440.	2.1	2
8	On the Breakdown Voltage Temperature Dependence of High-Voltage Power Diode Passivated with Diamond-Like Carbon. , 2021, , .		0
9	Modeling Nanoscale IIIâ€“V Channel MOSFETs with the Self-Consistent Multi-Valley/Multi-Subband Monte Carlo Approach. Electronics (Switzerland), 2021, 10, 2472.	3.1	0
10	New DG FeFET topology with enhanced SS and non-hysteretic behavior. Solid-State Electronics, 2020, 168, 107727.	1.4	0
11	Electron mobility of strained InGaAs long-channel MOSFETs: From scattering rates to TCAD model. Solid-State Electronics, 2020, 172, 107902.	1.4	1
12	TCAD Simulation Framework of Gas Desorption in CNT FET NO₂ Sensors. IEEE Transactions on Electron Devices, 2020, 67, 4682-4686.	3.0	2
13	TCAD Study of VLD Termination in Large-Area Power Devices Featuring a DLC Passivation. IEEE Transactions on Electron Devices, 2020, 67, 4645-4648.	3.0	1
14	Numerical Investigation of the Leakage Current and Blocking Capabilities of High-Power Diodes with Doped DLC Passivation Layers. , 2019, , .		1
15	TFET inverter static and transient performances in presence of traps and localized strain. Solid-State Electronics, 2019, 159, 38-42.	1.4	8
16	New DG FeFET architecture with enhanced SS and non-hysteretic behaviour. , 2019, , .		1
17	On the electron mobility of strained InGaAs channel MOSFETs. , 2019, , .		1
18	Electrical characterization of epoxy-based molding compounds for next generation HV ICs in presence of moisture. Microelectronics Reliability, 2018, 88-90, 752-755.	1.7	7

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19	Characterization of dielectric properties and conductivity in encapsulation materials with high insulating filler contents. IEEE Transactions on Dielectrics and Electrical Insulation, 2018, 25, 2421-2428.	2.9	8
20	TFET-based inverter performance in the presence of traps and localized strain. , 2018, , .		0
21	TCAD study of DLC coatings for large-area high-power diodes. Microelectronics Reliability, 2018, 88-90, 1094-1097.	1.7	3
22	3D TCAD modeling of NO<inf>2</inf>CNT FET sensors. , 2018, , .		2
23	Full-quantum modeling of III-V Tunnel-FETs architectures. Composants NanoÃ©lectroniques, 2018, 18, .	0.2	0
24	Role of the Insulating Fillers in the Encapsulation Material on the Lateral Charge Spreading in HV-ICs. IEEE Transactions on Electron Devices, 2017, 64, 1209-1216.	3.0	9
25	Investigation of the combined effect of traps and strain on optimized n- and p-type TFETs. , 2017, , .		1
26	Impact of Traps and Strain on Optimized n- and p-Type TFETs Integrated on the Same InAs/AlGaSb Technology Platform. IEEE Transactions on Electron Devices, 2017, 64, 3108-3113.	3.0	5
27	Design guidelines for GaSb/InAs TFET exploiting strain and device size. Solid-State Electronics, 2017, 129, 157-162.	1.4	12
28	Modelling nanoscale n-MOSFETs with III-V compound semiconductor channels: From advanced models for band structures, electrostatics and transport to TCAD. , 2017, , .		9
29	TCAD Mobility Model of III-V Short-Channel Double-Gate FETs Including Ballistic Corrections. IEEE Transactions on Electron Devices, 2017, 64, 4882-4888.	3.0	5
30	Impact of strain and interface traps on the performance of IIIâ€“V nanowire TFETs. , 2016, , .		0
31	TCAD-based investigation on transport properties of Diamond-like carbon coatings for HV-ICs. , 2016, , .		6
32	Optimization of GaSb/InAs TFET exploiting different strain configurations. , 2016, , .		2
33	Theoretical analysis and modeling for nanoelectronics. Solid-State Electronics, 2016, 125, 2-13.	1.4	6
34	Simulation of Graphene Base Transistors With Bilayer Tunnel Oxide Barrier: Model Calibration and Performance Projection. IEEE Electron Device Letters, 2016, 37, 1489-1492.	3.9	0
35	A full-quantum simulation study of InGaAs NW MOSFETs including interface traps. , 2016, , .		5
36	Performance study of strained IIIâ€“V materials for ultra-thin body transistor applications. , 2016, , .		3

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37	TCAD low-field mobility model for InGaAs UTB MOSFETs including quasi-ballistic corrections. , 2016, , .		3
38	Impact of bias conditions on electrical stress and ionizing radiation effects in Si-based TFETs. Solid-State Electronics, 2016, 115, 146-151.	1.4	6
39	Impact of Strain on Tunneling Current and Threshold Voltage in IIIâ€“V Nanowire TFETs. IEEE Electron Device Letters, 2016, 37, 560-563.	3.9	18
40	Comprehensive comparison and experimental validation of band-structure calculation methods in IIIâ€“V semiconductor quantum wells. Solid-State Electronics, 2016, 115, 92-102.	1.4	20
41	TCAD analysis of the leakage current and breakdown versus temperature of GaN-on-Silicon vertical structures. Solid-State Electronics, 2016, 115, 173-178.	1.4	8
42	Modeling the imaginary branch in III–V tunneling devices: Effective mass vs k · p. , 2015, , .		3
43	Influence of interface traps on the performance of Tunnel FETs. , 2015, , .		0
44	Modeling and characterization of hot-carrier stress degradation in power MOSFETs. , 2015, , .		0
45	Numerical investigation of the lateral and vertical leakage currents and breakdown regimes in GaN-on-Silicon vertical structures. , 2015, , .		21
46	Modeling approaches for band-structure calculation in III-V FET quantum wells. , 2015, , .		4
47	Effects of electrical stress and ionizing radiation on Si-based TFETs. , 2015, , .		2
48	A TCAD Low-Field Electron Mobility Model for Thin-Body InGaAs on InP MOSFETs Calibrated on Experimental Characteristics. IEEE Transactions on Electron Devices, 2015, 62, 3645-3652.	3.0	8
49	Theoretical analyses and modeling for nanoelectronics. , 2015, , .		1
50	Optimization of a Pocketed Dual-Metal-Gate TFET by Means of TCAD Simulations Accounting for Quantization-Induced Bandgap Widening. IEEE Transactions on Electron Devices, 2015, 62, 44-51.	3.0	48
51	Graphene base heterojunction transistor: An explorative study on device potential, optimization, and base parasitics. Solid-State Electronics, 2015, 114, 23-29.	1.4	7
52	Simulations of Graphene Base Transistors With Improved Graphene Interface Model. IEEE Electron Device Letters, 2015, 36, 969-971.	3.9	6
53	Capacitance estimation for InAs Tunnel FETs by means of full-quantum <mml:math xmlns:mml="http://www.w3.org/1998/Math/MathML" altimg="si58.gif" overflow="scroll"><mml:mrow><mml:mi mathvariant="bold">k</mml:mi><mml:mo>Â·</mml:mo><mml:mi mathvariant="bold">p</mml:mi></mml:mrow></mml:math> simulation. Solid-State Electronics, 2015, 108, 104-109.	1.4	13
54	Efficient quantum mechanical simulation of band-to-band tunneling. , 2015, , .		3

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55	Leakage current and breakdown of GaN-on-Silicon vertical structures. , 2015, , .		4
56	Analytical model of thin-body InGaAs-on-InP MOSFET low-field electron mobility for integration in TCAD tools. , 2015, , .		2
57	A quasi 2D semianalytical model for the potential profile in hetero and homojunction tunnel FETs. Solid-State Electronics, 2015, 113, 86-91.	1.4	5
58	Effects of D<inf>it</inf>-induced degradation on InGaAs/InAlAs Nanowire Superlattice-FET using Al<inf>2</inf>O<inf>3</inf> and HfO<inf>2</inf>/La<inf>2</inf>O<inf>3</inf> as gate stacks. , 2015, , .		2
59	Graphene-base heterojunction transistors for post-CMOS high-speed applications: Hopes and challenges. , 2015, , .		1
60	Investigation of Hot Carrier Stress and Constant Voltage Stress in High- <inline-formula> <tex-math notation="LaTeX">$kappa$</tex-math></inline-formula> Si-Based TFETs. IEEE Transactions on Device and Materials Reliability, 2015, 15, 236-241.	2.0	14
61	Role of encapsulation formulation on charge transport phenomena and HV device instability. , 2015, , .		4
62	Optimization of HV LDMOS devices accounting for packaging interaction. , 2015, , .		8
63	Numerical study of GaN-on-Si HEMT breakdown instability accounting for substrate and packaging interactions. , 2015, , .		3
64	Theoretical analyses and modeling for nanoelectronics. , 2015, , .		1
65	Characterization and Modeling of High-Voltage LDMOS Transistors. , 2015, , 309-339.		2
66	Total Ionizing Dose Effects in Si-Based Tunnel FETs. IEEE Transactions on Nuclear Science, 2014, 61, 2874-2880.	2.0	15
67	Capacitance estimation for InAs Tunnel FETs by means of full-quantum k·p simulation. , 2014, , .		1
68	A quasi 2D semianalytical model for the potential profile in hetero and homojunction tunnel FETs. , 2014, , .		4
69	TCAD modeling of charge transport in HV-IC encapsulation materials. , 2014, , .		9
70	TCAD analysis of HCS degradation in LDMOS devices under AC stress conditions. , 2014, , .		1
71	Impact of crystallographic orientation and impurity scattering in Graphene-Base Heterojunction Transistors for Terahertz Operation. , 2014, , .		2
72	Investigation on the electrical properties of superlattice FETs using a non-parabolic band model. Solid-State Electronics, 2014, 98, 45-49.	1.4	3

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73	Exploiting Negative Differential Resistance in Monolayer Graphene FETs for High Voltage Gains. IEEE Transactions on Electron Devices, 2014, 61, 617-624.	3.0	13
74	Dual-Metal-Gate InAs Tunnel FET With Enhanced Turn-On Steepness and High On-Current. IEEE Transactions on Electron Devices, 2014, 61, 776-784.	3.0	79
75	TFET Inverters With n-/p-Devices on the Same Technology Platform for Low-Voltage/Low-Power Applications. IEEE Transactions on Electron Devices, 2014, 61, 473-478.	3.0	47
76	Semianalytical quantum model for graphene field-effect transistors. Journal of Applied Physics, 2014, 116, .	2.5	3
77	Linear drain current degradation of STI-based LDMOS transistors under AC stress conditions. , 2014, , .		1
78	Optimization of n- and p-type TFETs Integrated on the Same ${m InAs}/{m Al}_{x}{m Ga}_{1-x}{m Sb}$ Technology Platform. IEEE Transactions on Electron Devices, 2014, 61, 178-185.	3.0	46
79	Boosting the voltage gain of graphene FETs through a differential amplifier scheme with positive feedback. Solid-State Electronics, 2014, 100, 54-60.	1.4	7
80	Characterization and modeling of electrical stress degradation in STI-based integrated power devices. Solid-State Electronics, 2014, 102, 25-41.	1.4	79
81	Design and optimization of impurity- and electrostatically-doped superlattice FETs to meet all the ITRS power targets at VDD=0.4V. Solid-State Electronics, 2014, 101, 70-78.	1.4	8
82	TCAD modeling of encapsulation layer in high-voltage, high-temperature operation regime. , 2014, , .		6
83	Effects of bias on the radiation responses of Si-based TFETs. , 2014, , .		1
84	Deterministic solution of the 1D Boltzmann transport equation: Application to the study of current transport in nanowire FETs. Microelectronics Journal, 2013, 44, 20-25.	2.0	2
85	Graphene Base Transistors: A Simulation Study of DC and Small-Signal Operation. IEEE Transactions on Electron Devices, 2013, 60, 3584-3591.	3.0	23
86	TCAD Simulation of Hot-Carrier and Thermal Degradation in STI-LDMOS Transistors. IEEE Transactions on Electron Devices, 2013, 60, 691-698.	3.0	112
87	Gate stack optimization to minimize power consumption in super-lattice fets. , 2013, , .		1
88	Non-parabolic band effects on the electrical properties of superlattice FETs. , 2013, , .		5
89	DC and small-signal numerical simulation of graphene base transistor for terahertz operation. , 2013, , .		5
90	Modeling and characterization of hot-carrier stress degradation in power MOSFETs (invited). , 2013, , .		2

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91	Semianalytical Model of the Subthreshold Current in Short-Channel Junctionless Symmetric Double-Gate Field-Effect Transistors. IEEE Transactions on Electron Devices, 2013, 60, 1342-1348.	3.0	115
92	Full-quantum simulation of heterojunction TFET inverters providing better performance than multi-gate CMOS at sub-0.35V V<inf>DD</inf>. , 2013, , .		0
93	Mode space approach for tight-binding transport simulations in graphene nanoribbon field-effect transistors including phonon scattering. Journal of Applied Physics, 2013, 113, 144506.	2.5	8
94	Drain-conductance optimization in nanowire TFETs by means of a physics-based analytical model. Solid-State Electronics, 2013, 84, 96-102.	1.4	45
95	Graphene-Base Heterojunction Transistor: An Attractive Device for Terahertz Operation. IEEE Transactions on Electron Devices, 2013, 60, 4263-4268.	3.0	39
96	Complementary n- and p-type TFETs on the same InAs/Al<inf>0.05</inf>Ga<inf>0.95</inf>Sb platform. , 2013, , .		4
97	TCAD predictions of linear and saturation HCS degradation in STI-based LDMOS transistors stressed in the impact-ionization regime. , 2013, , .		9
98	Boosting InAs TFET on-current above 1 mA/μm with no leakage penalty. , 2013, , .		1
99	Can Interface Traps Suppress TFET Ambipolarity?. IEEE Electron Device Letters, 2013, 34, 1557-1559.	3.9	34
100	Optimization of staggered heterojunction p-TFETs for LSTP and LOP applications. , 2013, , .		2
101	TCAD degradation modeling for LDMOS transistors. , 2012, , .		3
102	Analysis of Threshold Voltage Variability Due to Random Dopant Fluctuations in Junctionless FETs. IEEE Electron Device Letters, 2012, 33, 336-338.	3.9	139
103	Physics-based analytical model of nanowire tunnel-FETs. , 2012, , .		0
104	Drain-conductance optimization in nanowire TFETs. , 2012, , .		12
105	Numerical investigation on the junctionless nanowire FET. Solid-State Electronics, 2012, 71, 13-18.	1.4	14
106	Optimization and Analysis of the Dual n/p-LDMOS Device. IEEE Transactions on Electron Devices, 2012, 59, 745-753.	3.0	11
107	Physical Model of the Junctionless UTB SOI-FET. IEEE Transactions on Electron Devices, 2012, 59, 941-948.	3.0	56
108	Temperature Dependence of the Threshold Voltage Shift Induced by Carrier Injection in Integrated STI-Based LDMOS Transistors. IEEE Electron Device Letters, 2011, 32, 791-793.	3.9	15

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109	TCAD optimization of a dual N/P-LDMOS transistor. , 2011, , .		2
110	An investigation on steep-slope and low-power nanowire FETs. , 2011, , .		1
111	Performance limits of superlattice-based steep-slope nanowire FETs. , 2011, , .		15
112	Junction-less stackable SONOS memory realized on vertical-Si-nanowire for 3-D application. , 2011, , .		6
113	A quasi-analytical model of the junctionless nanowire field-effect transistor. , 2011, , .		0
114	Junction-Less Stackable SONOS Memory Realized on Vertical-Si-Nanowire for 3-D Application. , 2011, , .		1
115	Mode Space Approach for Tight Binding Transport Simulation in Graphene Nanoribbon FETs. IEEE Nanotechnology Magazine, 2011, 10, 371-378.	2.0	17
116	Full understanding of hot-carrier-induced degradation in STI-based LDMOS transistors in the impact-ionization operating regime. , 2011, , .		21
117	Numerical investigation on the junctionless nanowire FET. , 2011, , .		16
118	Hot-carrier stress induced degradation in Multi-STI-Finger LDMOS: An experimental and numerical insight. Solid-State Electronics, 2011, 65-66, 57-63.	1.4	12
119	Steep-slope nanowire FET with a superlattice in the source extension. Solid-State Electronics, 2011, 65-66, 108-113.	1.4	13
120	Vertical-Si-Nanowire-Based Nonvolatile Memory Devices With Improved Performance and Reduced Process Complexity. IEEE Transactions on Electron Devices, 2011, 58, 1329-1335.	3.0	33
121	Theory of the Junctionless Nanowire FET. IEEE Transactions on Electron Devices, 2011, 58, 2903-2910.	3.0	204
122	Physics-Based Analytical Model for HCS Degradation in STI-LDMOS Transistors. IEEE Transactions on Electron Devices, 2011, 58, 3072-3080.	3.0	84
123	Investigation on superlattice heterostructures for steep-slope nanowire FETs. , 2011, , .		4
124	High-frequency analog GNR-FET design criteria. , 2011, , .		4
125	Effective Mobility in Nanowire FETs Under Quasi-Ballistic Conditions. IEEE Transactions on Electron Devices, 2010, 57, 336-344.	3.0	34
126	A Low-Field Mobility Model for Bulk, Ultrathin Body SOI and Double-Gate n-MOSFETs With Different Surface and Channel Orientationsâ€"Part I: Fundamental Principles. IEEE Transactions on Electron Devices, 2010, 57, 1567-1574.	3.0	11

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127	A Low-Field Mobility Model for Bulk, Ultrathin Body SOI and Double-Gate n-MOSFETs With Different Surface and Channel Orientationsâ€"Part II: Ultrathin Silicon Films. IEEE Transactions on Electron Devices, 2010, 57, 1575-1582.	3.0	8
128	A Low-Field Mobility Model for Bulk and Ultrathin-Body SOI p-MOSFETs With Different Surface and Channel Orientations. IEEE Transactions on Electron Devices, 2010, 57, 3287-3294.	3.0	2
129	Theoretical analysis of the vertical LOCOS DMOS transistor with process-induced stress enhancement. Solid-State Electronics, 2010, 54, 950-956.	1.4	5
130	Modeling of gate-all-around charge trapping SONOS memory cells. Solid-State Electronics, 2010, 54, 997-1002.	1.4	20
131	Superlattice-based steep-slope switch. , 2010, , .		0
132	Steep-slope nanowire FET with a superlattice in the source extension. , 2010, , .		5
133	Improving the accuracy of the Schrödinger-Poisson solution in CNWs and CNTs. , 2010, , .		4
134	Computational study of graphene nanoribbon FETs for RF applications. , 2010, , .		17
135	Hot-carrier stress induced degradation in Multi-STI-Finger LDMOS: An experimental and numerical insight. , 2010, , .		1
136	Steep-slope nanowire field-effect transistor (SS-NWFET). , 2010, , .		1
137	Analysis of HCS in STI-based LDMOS transistors. , 2010, , .		18
138	Numerical investigation of the total SOA of trench field-plate LDMOS devices. , 2010, , .		8
139	Performance analysis of nonvolatile gate-all-around charge-trapping TAHOS memory cells. , 2009, , .		0
140	Investigation on saturation effects in the rugged LDMOS transistor. Power Semiconductor Devices & IC's, 2009 ISPSD 2009 21st International Symposium on, 2009, , .	0.0	10
141	Explanation of the Rugged LDMOS Behavior by Means of Numerical Analysis. IEEE Transactions on Electron Devices, 2009, 56, 2811-2818.	3.0	37
142	Tight-binding and effective mass modeling of armchair graphene nanoribbon FETs. Solid-State Electronics, 2009, 53, 462-467.	1.4	39
143	An investigation of performance limits of conventional andÂtunneling graphene-based transistors. Journal of Computational Electronics, 2009, 8, 441-450.	2.5	12
144	Mode Space Approach for Tight-Binding Transport Simulation in Graphene Nanoribbon FETs. , 2009, , .		2

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145	An Investigation on Effective Mobility in Nanowire FETs under Quasi-Ballistic Conditions. , 2009, , .		1
146	Ballistic ratio and backscattering coefficient in short-channel NW-FETs. , 2009, , .		2
147	Modeling of nonvolatile gate-all-around charge-trapping SONOS memory cells. , 2009, , .		3
148	Theoretical analysis of the vertical LOCOS DMOS transistor with process-induced stress enhancement. , 2009, , .		0
149	Simulation study of graphene nanoribbon tunneling transistors including edge roughness effects. , 2009, , .		2
150	Impact-ionization coefficient in silicon at high fieldsâ€" aÂparametric approach. Journal of Computational Electronics, 2008, 7, 151-154.	2.5	3
151	Semiclassical transport in silicon nanowire FETs including surface roughness. Journal of Computational Electronics, 2008, 7, 355-358.	2.5	22
152	Theoretical foundations of the quantum drift-diffusion and density-gradient models. Solid-State Electronics, 2008, 52, 526-532.	1.4	25
153	Phonon-scattering effects in CNT-FETs with different dimensions and dielectric materials. Solid-State Electronics, 2008, 52, 1329-1335.	1.4	4
154	Computational Study of the Ultimate Scaling Limits of CNT Tunneling Devices. IEEE Transactions on Electron Devices, 2008, 55, 313-321.	3.0	38
155	Quasi-Ballistic Transport in Nanowire Field-Effect Transistors. IEEE Transactions on Electron Devices, 2008, 55, 2918-2930.	3.0	41
156	Investigation of the Transport Properties of Silicon Nanowires Using Deterministic and Monte Carlo Approaches to the Solution of the Boltzmann Transport Equation. IEEE Transactions on Electron Devices, 2008, 55, 2086-2096.	3.0	90
157	Quasi-ballistic transport in nanowire field-effect transistors. , 2008, , .		4
158	Tight-binding and effective mass modeling of armchair carbon nanoribbon FETs. , 2008, , .		1
159	Si-Nanowire Based Gate-All-Around Nonvolatile SONOS Memory Cell. IEEE Electron Device Letters, 2008, 29, 518-521.	3.9	77
160	OH dangling-bond saturation and dielectric function effects in ultra-scaled SNW-FETs. , 2008, , .		0
161	Unified model for low-field electron mobility in bulk and SOI-MOSFETs with different substrate orientations and its application to quantum drift-diffusion simulation. , 2008, , .		2
162	Graphene nanoribbons FETs for high-performance logic applications: Perspectives and challenges. , 2008, , .		5

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163	Hierarchical modeling of carbon nanoribbon devices for CNR-FETs engineering. , 2008, , .		2
164	Band Effects on the Transport Characteristics of Ultrascaled SNW-FETs. IEEE Nanotechnology Magazine, 2008, 7, 700-709.	2.0	17
165	Effects of Channel Orientations, High-? Gate Stacks and Stress on UTB-FETs: A QDD Simulation Study. , 2008, , .		0
166	Physically-based unified compact model for low-field carrier mobility in MOSFETs with different gate stacks and biaxial/uniaxial stress conditions. , 2007, , .		3
167	Effects of High-$kappa$ (HfO$_2$) Gate Dielectrics in Double-Gate and Cylindrical-Nanowire FETs Scaled to the Ultimate Technology Nodes. IEEE Nanotechnology Magazine, 2007, 6, 90-96.	2.0	28
168	Band Structure Effects on the Current-Voltage Characteristics of SNW-FETs. , 2007, , .		3
169	Comparison of Device Performance and Scaling Properties of Cylindrical-Nanowire (CNW) and Carbon-Nanotube (CNT) Transistors. AIP Conference Proceedings, 2007, , .	0.4	1
170	Low-Field Electron Mobility Model for Ultrathin-Body SOI and Double-Gate MOSFETs With Extremely Small Silicon Thicknesses. IEEE Transactions on Electron Devices, 2007, 54, 2204-2212.	3.0	67
171	Band-Structure Effects in Ultrascaled Silicon Nanowires. IEEE Transactions on Electron Devices, 2007, 54, 2243-2254.	3.0	74
172	Extension of the R-Îİ method to any order. Journal of Computational Electronics, 2007, 6, 251-254.	2.5	0
173	Experimental Investigation on Carrier Dynamics at the Thermal Breakdown. AIP Conference Proceedings, 2007, , .	0.4	0
174	Effects of the Band-Structure Modification in Silicon Nanowires with Small Diameters. Solid-State Device Research Conference, 2008 ESSDERC 2008 38th European, 2006, , .	0.0	11
175	Comparison of device performance and scaling properties of cylindrical-nanowire (CNW) and carbon-nanotube (CNT) transistors. , 2006, , .		2
176	Investigating the performance limits of silicon-nanowire and carbon-nanotube FETs. Solid-State Electronics, 2006, 50, 78-85.	1.4	48
177	Quantum-mechanical analysis of the electrostatics in silicon-nanowire and carbon-nanotube FETs. Solid-State Electronics, 2006, 50, 709-715.	1.4	21
178	Theory and experimental validation of a new analytical model for the position-dependent Hall Voltage in devices with arbitrary aspect ratio. IEEE Transactions on Electron Devices, 2006, 53, 314-322.	3.0	8
179	The R-Îİ Approach to Tunnelling in Nanoscale Devices. , 2006, , 175-178.		0
180	Measurement and modeling of the electron impact-ionization coefficient in silicon up to very high temperatures. IEEE Transactions on Electron Devices, 2005, 52, 2290-2299.	3.0	43

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181	On the Electrostatics of Double-Gate and Cylindrical Nanowire MOSFETs. Journal of Computational Electronics, 2005, 4, 71-74.	2.5	11
182	A Coherent Extension of the Transport Equations in Semiconductors Incorporating the Quantum Correctionâ€"Part I: Single-Particle Dynamics. IEEE Nanotechnology Magazine, 2005, 4, 495-502.	2.0	6
183	A Quantum-Mechanical Analysis of the Electrostatics in Multiple-Gate FETs. , 2005, , .		2
184	A Coherent Extension of the Transport Equations in Semiconductors Incorporating the Quantum Correctionâ€"Part II: Collective Transport. IEEE Nanotechnology Magazine, 2005, 4, 503-509.	2.0	6
185	A new numerical and experimental analysis tool for ESD devices by means of the transient interferometric technique. IEEE Electron Device Letters, 2005, 26, 916-918.	3.9	11
186	The Density-Gradient Correction as a Disguised Pilot Wave of de Broglie. , 2004, , 13-16.		4
187	Hole density of states and group velocity inSiO2. Physical Review B, 2003, 68, .	3.2	0
188	Extraction Method for the Impact-Ionization Multiplication Factor in Silicon at Large Operating Temperatures. , 2002, , .		14
189	Automatic 2-D and 3-D simulation of parasitic structures in smart-power integrated circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2002, 21, 791-798.	2.7	7
190	Density of states and group velocity of electrons inSiO2calculated from a full band structure. Physical Review B, 2002, 66, .	3.2	27
191	Full-band transport properties of silicon dioxide using the spherical-harmonics expansion of the BTE. Physica B: Condensed Matter, 2002, 314, 193-197.	2.7	5
192	Density of States and Group Velocity Calculations for SiO2. , 2001, , 50-53.		0
193	Band-structure calculations of SiO/sub 2/ by means of Hartree-Fock and density-functional techniques. IEEE Transactions on Electron Devices, 2000, 47, 1795-1803.	3.0	44
194	Determination of the Hall voltage in devices with arbitrary aspect ratio and probe position. , 0, , .		2
195	Experimental extraction of the electron impact-ionization coefficient at large operating temperatures. , 0, , .		17
196	A new approach to the self-consistent solution of the Schrodinger-Poisson equations in nanowire MOSFETs. , 0, , .		17
197	Investigation about the high-temperature impact-ionization coefficient in silicon. , 0, , .		17
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