

# Krishnendu Chakrabarty

## List of Publications by Citations

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687  
papers

10,850  
citations

46  
h-index

80  
g-index

790  
ext. papers

13,221  
ext. citations

2.3  
avg, IF

6.88  
L-index

#	Paper	IF	Citations
687	Grid coverage for surveillance and target location in distributed sensor networks. <i>IEEE Transactions on Computers</i> , <b>2002</b> , 51, 1448-1453	2.5	599
686	Sensor deployment and target localization based on virtual forces <b>2003</b> ,		497
685	Sensor deployment and target localization in distributed sensor networks. <i>Transactions on Embedded Computing Systems</i> , <b>2004</b> , 3, 61-91	1.8	325
684	On a new class of codes for identifying vertices in graphs. <i>IEEE Transactions on Information Theory</i> , <b>1998</b> , 44, 599-611	2.8	243
683	Test Challenges for 3D Integrated Circuits. <i>IEEE Design and Test of Computers</i> , <b>2009</b> , 26, 26-35		209
682	Test Wrapper and Test Access Mechanism Co-Optimization for System-on-Chip. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>2002</b> , 18, 213-230	0.7	184
681	A distributed coverage- and connectivity-centric technique for selecting active nodes in wireless sensor networks. <i>IEEE Transactions on Computers</i> , <b>2005</b> , 54, 978-991	2.5	176
680	On computing mobile agent routes for data fusion in distributed sensor networks. <i>IEEE Transactions on Knowledge and Data Engineering</i> , <b>2004</b> , 16, 740-753	4.2	155
679	Test data compression and test resource partitioning for system-on-a-chip using frequency-directed run-length (FDR) codes. <i>IEEE Transactions on Computers</i> , <b>2003</b> , 52, 1076-1088	2.5	143
678	High-level synthesis of digital microfluidic biochips. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , <b>2008</b> , 3, 1-32	1.7	141
677	Unified high-level synthesis and module placement for defect-tolerant microfluidic biochips <b>2005</b> ,		123
676	Uncertainty-aware and coverage-oriented deployment for sensor networks. <i>Journal of Parallel and Distributed Computing</i> , <b>2004</b> , 64, 788-798	4.4	120
675	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2013</b> , 32, 59-72	2.5	106
674	Distributed sensor networks—review of recent research. <i>Journal of the Franklin Institute</i> , <b>2001</b> , 338, 655-668	4	103
673	Nine-coded compression technique for testing embedded cores in SoCs. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2005</b> , 13, 719-731	2.6	96
672	. <i>IEEE Journal on Selected Areas in Communications</i> , <b>2011</b> , 29, 582-594	14.2	91
671	Optimization of Dilution and Mixing of Biochemical Samples Using Digital Microfluidic Biochips. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2010</b> , 29, 1696-1708	2.5	91

670	Broadcast electrode-addressing for pin-constrained multi-functional digital microfluidic biochips <b>2008</b> ,			87
669	. <i>IEEE Transactions on Reliability</i> , <b>2005</b> , 54, 145-155	4.6		87
668	Module placement for fault-tolerant microfluidics-based biochips. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2006</b> , 11, 682-710	1.5		81
667	Test access mechanism optimization, test scheduling, and tester data volume reduction for system-on-chip. <i>IEEE Transactions on Computers</i> , <b>2003</b> , 52, 1619-1631	2.5		77
666	Parallel scan-like test and multiple-defect diagnosis for digital microfluidic biochips. <i>IEEE Transactions on Biomedical Circuits and Systems</i> , <b>2007</b> , 1, 148-58	5.1		72
665	Pre-bond probing of TSVs in 3D stacked ICs <b>2011</b> ,			71
664	TSV open defects in 3D integrated circuits <b>2012</b> ,			70
663	Location-aided flooding: an energy-efficient data dissemination protocol for wireless-sensor networks. <i>IEEE Transactions on Computers</i> , <b>2005</b> , 54, 36-46	2.5		69
662	Optimal test access architectures for system-on-a-chip. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2001</b> , 6, 26-49	1.5		69
661	Distributed Mobility Management for Target Tracking in Mobile Sensor Networks. <i>IEEE Transactions on Mobile Computing</i> , <b>2007</b> , 6, 872-887	4.6		67
660	Board-Level Functional Fault Diagnosis Using Artificial Neural Networks, Support-Vector Machines, and Weighted-Majority Voting. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2013</b> , 32, 723-736	2.5		65
659	Cross-Contamination Avoidance for Droplet Routing in Digital Microfluidic Biochips. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2012</b> , 31, 817-830	2.5		65
658	Integrated control-path design and error recovery in the synthesis of digital microfluidic lab-on-chip. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , <b>2010</b> , 6, 1-28	1.7		64
657	Digital Microfluidic Biochips <b>2006</b> ,			63
656	. <i>IEEE Sensors Journal</i> , <b>2005</b> , 5, 763-773	4		60
655	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2008</b> , 16, 432-443	2.6		59
654	Keynote Paper: From EDA to IoT eHealth: Promises, Challenges, and Solutions. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2018</b> , 37, 2965-2978	2.5		57
653	Design Tools for Digital Microfluidic Biochips: Toward Functional Diversification and More Than Moore. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2010</b> , 29, 1001-1017	2.5		56

652	Design of system-on-a-chip test access architectures under place-and-route and power constraints <b>2000,</b>		56
651	Fault-Tolerant Training with On-Line Fault Detection for RRAM-Based Neural Computing Systems <b>2017,</b>		55
650	Test-access mechanism optimization for core-based three-dimensional SOCs <b>2008,</b>		55
649	Test data compression using dictionaries with selective entries and fixed-length indices. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2003</b> , 8, 470-490	1.5	54
648	Digital Microfluidic Biochips		52
647	Droplet-trace-based array partitioning and a pin assignment algorithm for the automated design of digital microfluidic biochips <b>2006,</b>		51
646	Combining low-power scan testing and test data compression for system-on-a-chip <b>2001,</b>		51
645	Testing of Flow-Based Microfluidic Biochips: Fault Modeling, Test Generation, and Experimental Demonstration. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2014</b> , 33, 1463-1475	2.5	48
644	Testing and Diagnosis of Realistic Defects in Digital Microfluidic Biochips. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>2007</b> , 23, 219-233	0.7	48
643	Layout-driven test-architecture design and optimization for 3D SoCs under pre-bond test-pin-count constraint <b>2009,</b>		46
642	Test-Pattern Grading and Pattern Selection for Small-Delay Defects. <i>VLSI Test Symposium (VTS), Proceedings, IEEE</i> , <b>2008,</b>		46
641	Stuck-at Fault Tolerance in RRAM Computing Systems. <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , <b>2018</b> , 8, 102-115	5.2	46
640	Test-Pattern Selection for Screening Small-Delay Defects in Very-Deep Submicrometer Integrated Circuits. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2010</b> , 29, 760-773 <sup>2.5</sup>		45
639	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2010</b> , 29, 552-565	2.5	44
638	Privacy-Preserving Detection of Sybil Attacks in Vehicular Ad Hoc Networks <b>2007,</b>		44
637	Pruning-based, energy-optimal, deterministic I/O device scheduling for hard real-time systems. <i>Transactions on Embedded Computing Systems</i> , <b>2005</b> , 4, 141-167	1.8	44
636	Design-Space Exploration and Optimization of an Energy-Efficient and Reliable 3-D Small-World Network-on-Chip. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2017</b> , 36, 719-732	2.5	43
635	Digital microfluidic biochips: A vision for functional diversity and more than moore <b>2010,</b>		42

634	High-level synthesis for micro-electrode-dot-array digital microfluidic biochips <b>2016</b> ,		41
633	Security Assessment of Cyberphysical Digital Microfluidic Biochips. <i>IEEE/ACM Transactions on Computational Biology and Bioinformatics</i> , <b>2016</b> , 13, 445-58	3	41
632	Test-Architecture Optimization and Test Scheduling for TSV-Based 3-D Stacked ICs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2011</b> , 30, 1705-1718	2.5	41
631	Fault modeling and functional test methods for digital microfluidic biochips. <i>IEEE Transactions on Biomedical Circuits and Systems</i> , <b>2009</b> , 3, 241-53	5.1	41
630	Test-architecture optimization for TSV-based 3D stacked ICs <b>2010</b> ,		40
629	Optimization methods for post-bond die-internal/external testing in 3D stacked ICs <b>2010</b> ,		39
628	Dynamic adaptation for fault tolerance and power management in embedded real-time systems. <i>Transactions on Embedded Computing Systems</i> , <b>2004</b> , 3, 336-360	1.8	38
627	Fault detection, real-time error recovery, and experimental demonstration for digital microfluidic biochips <b>2013</b> ,		37
626	Digital microfluidic biochips <b>2011</b> ,		37
625	Automated design of pin-constrained digital microfluidic biochips under droplet-interference constraints. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , <b>2007</b> , 3, 14	1.7	37
624	Control-Layer Routing and Control-Pin Minimization for Flow-Based Microfluidic Biochips. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2017</b> , 36, 55-68	2.5	36
623	Droplet Size-Aware High-Level Synthesis for Micro-Electrode-Dot-Array Digital Microfluidic Biochips. <i>IEEE Transactions on Biomedical Circuits and Systems</i> , <b>2017</b> , 11, 612-626	5.1	36
622	Secure Randomized Checkpointing for Digital Microfluidic Biochips. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2018</b> , 37, 1119-1132	2.5	36
621	Cost-effective integration of three-dimensional (3D) ICs emphasizing testing cost analysis <b>2010</b> ,		36
620	. <i>Computer</i> , <b>2016</b> , 49, 36-43	1.6	35
619	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2017</b> , 36, 733-746	2.5	35
618	Contactless Pre-Bond TSV Test and Diagnosis Using Ring Oscillators and Multiple Voltage Levels. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2014</b> , 33, 774-785	2.5	34
617	Board-Level Functional Fault Diagnosis Using Multikernel Support Vector Machines and Incremental Learning. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2014</b> , 33, 279-290	2.5	34

616	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2008</b> , 27, 1905-1917	2.5	33
615	Interconnect-Aware and Layout-Oriented Test-Pattern Selection for Small-Delay Defects <b>2008</b> ,		33
614	Real-time task scheduling for energy-aware embedded systems. <i>Journal of the Franklin Institute</i> , <b>2001</b> , 338, 729-750	4	33
613	Machine Learning for Hardware Security: Opportunities and Risks. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>2018</b> , 34, 183-201	0.7	32
612	. <i>IEEE Transactions on Computers</i> , <b>2016</b> , 65, 2767-2779	2.5	32
611	Test-wrapper optimization for embedded cores in TSV-based three-dimensional SOCs <b>2009</b> ,		32
610	Testing of SoCs with Hierarchical Cores: Common Fallacies, Test Access Optimization, and Test Scheduling. <i>IEEE Transactions on Computers</i> , <b>2009</b> , 58, 409-423	2.5	32
609	Introduction to DAC 2007 special section. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , <b>2008</b> , 4, 1-2	1.7	32
608	Concurrent testing of digital microfluidics-based biochips. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2006</b> , 11, 442-464	1.5	32
607	Design automation for microfluidics-based biochips. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , <b>2005</b> , 1, 186-223	1.7	32
606	Test Planning and Test Resource Optimization for Droplet-Based Microfluidic Systems. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>2006</b> , 22, 199-210	0.7	32
605	Broadcast Electrode-Addressing and Scheduling Methods for Pin-Constrained Digital Microfluidic Biochips. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2011</b> , 30, 986-999 <sup>5</sup>		31
604	Layout-Aware Solution Preparation for Biochemical Analysis on a Digital Microfluidic Biochip <b>2011</b> ,		31
603	Microfluidic encryption of on-chip biochemical assays <b>2016</b> ,		31
602	Real-Time Error Recovery in Cyberphysical Digital-Microfluidic Biochips Using a Compact Dictionary. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2013</b> , 32, 1839-1852	2.5	30
601	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2014</b> , 33, 1131-1144	2.5	29
600	Biochip Synthesis and Dynamic Error Recovery for Sample Preparation Using Digital Microfluidics. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2014</b> , 33, 183-196	2.5	29
599	TSV defects and TSV-induced circuit failures: The third dimension in test and design-for-test <b>2012</b> ,		29

598	Synchronization of washing operations with droplet routing for cross-contamination avoidance in digital microfluidic biochips <b>2010</b> ,		29
597	. <i>IEEE Design and Test of Computers</i> , <b>2008</b> , 25, 372-381		29
596	Error-Correcting Sample Preparation with Cyberphysical Digital Microfluidic Lab-on-Chip. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2016</b> , 22, 1-29	1.5	29
595	Cooling of integrated circuits using droplet-based microfluidics <b>2003</b> ,		29
594	Optimal zero-aliasing space compaction of test responses. <i>IEEE Transactions on Computers</i> , <b>1998</b> , 47, 1171-1187	2.5	28
593	Deterministic Built-in Pattern Generation for Sequential Circuits. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>1999</b> , 15, 97-114	0.7	28
592	Reliability-oriented broadcast electrode-addressing for pin-constrained digital microfluidic biochips <b>2011</b> ,		27
591	On-Chip Sample Preparation with Multiple Dilutions Using Digital Microfluidics <b>2012</b> ,		27
590	Exact routing for micro-electrode-dot-array digital microfluidic biochips <b>2017</b> ,		26
589	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2015</b> , 34, 29-42	2.5	26
588	Design methodology for sample preparation on digital microfluidic biochips <b>2012</b> ,		26
587	Error recovery in a micro-electrode-dot-array digital microfluidic biochip? <b>2016</b> ,		26
586	Towards fault-tolerant digital microfluidic lab-on-chip: Defects, fault modeling, testing, and reconfiguration <b>2008</b> ,		25
585	Optimizing 3D NoC design for energy efficiency: A machine learning approach <b>2015</b> ,		24
584	Digital Microfluidic Logic Gates and Their Application to Built-in Self-Test of Lab-on-Chip. <i>IEEE Transactions on Biomedical Circuits and Systems</i> , <b>2010</b> , 4, 250-62	5.1	24
583	Board-level fault diagnosis using Bayesian inference <b>2010</b> ,		24
582	Dictionary-based error recovery in cyberphysical digital-microfluidic biochips <b>2012</b> ,		24
581	Integrated droplet routing and defect tolerance in the synthesis of digital microfluidic biochips. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , <b>2008</b> , 4, 1-24	1.7	24

580	A Cross-Referencing-Based Droplet Manipulation Method for High-Throughput and Pin-Constrained Digital Microfluidic Arrays <b>2007</b> ,		24
579	Locking of biochemical assays for digital microfluidic biochips <b>2018</b> ,		23
578	. <i>IEEE Transactions on Multi-Scale Computing Systems</i> , <b>2015</b> , 1, 46-58		23
577	Control-layer optimization for flow-based mVLSI microfluidic biochips <b>2014</b> ,		23
576	Adaptive Board-Level Functional Fault Diagnosis Using Decision Trees <b>2012</b> ,		23
575	On effective and efficient in-field TSV repair for stacked 3D ICs <b>2013</b> ,		23
574	Design of Pin-Constrained General-Purpose Digital Microfluidic Biochips. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2013</b> , 32, 1307-1320	2.5	23
573	Smart diagnosis: Efficient board-level diagnosis and repair using artificial neural networks <b>2011</b> ,		23
572	Scan-chain design and optimization for three-dimensional integrated circuits. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , <b>2009</b> , 5, 1-26	1.7	23
571	Acoustic streaming vortices enable contactless, digital control of droplets. <i>Science Advances</i> , <b>2020</b> , 6, eaba0606	14.3	22
570	A general and exact routing methodology for Digital Microfluidic Biochips <b>2015</b> ,		22
569	On-chip biochemical sample preparation using digital microfluidics <b>2011</b> ,		22
568	Test-access mechanism optimization for core-based three-dimensional SOCs. <i>Microelectronics Journal</i> , <b>2010</b> , 41, 601-615	1.8	22
567	Healthcare IoT <b>2020</b> , 515-545		22
566	Efficient and Adaptive Error Recovery in a Micro-Electrode-Dot-Array Digital Microfluidic Biochip. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2018</b> , 37, 601-614	2.5	22
565	Non-invasive pre-bond TSV test using ring oscillators and multiple voltage levels <b>2013</b> ,		21
564	Testing microfluidic Fully Programmable Valve Arrays (FPVAs) <b>2017</b> ,		21
563	Test Schedule Optimization for Multicore SoCs: Handling Dynamic Voltage Scaling and Multiple Voltage Islands. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2012</b> , 31, 1754-1766	2.5	21



562	Identification of Defective TSVs in Pre-Bond Testing of 3D ICs <b>2011,</b>		21
561	Yield enhancement of reconfigurable microfluidics-based biochips using interstitial redundancy. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , <b>2006</b> , 2, 104-128	1.7	21
560	Fault-Tolerant Training Enabled by On-Line Fault Detection for RRAM-Based Neural Computing Systems. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2019</b> , 38, 1611-1624	2.5	20
559	Security implications of cyberphysical digital microfluidic biochips <b>2015,</b>		20
558	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2016</b> , 35, 985-998	2.5	19
557	Contactless, programmable acoustofluidic manipulation of objects on water. <i>Lab on A Chip</i> , <b>2019</b> , 19, 3397-3404	7.2	19
556	Optimization Methods for Post-Bond Testing of 3D Stacked ICs. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>2012</b> , 28, 103-120	0.7	19
555	<b>2017,</b>		19
554	Defect-aware high-level synthesis and module placement for microfluidic biochips. <i>IEEE Transactions on Biomedical Circuits and Systems</i> , <b>2008</b> , 2, 50-62	5.1	19
553	Cycle-Accurate Test Power Modeling and Its Application to SoC Test Architecture Design and Scheduling. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2008</b> , 27, 973-977	2.5	19
552	Micro-Electro-Dot-Array Digital Microfluidic Biochips: Technology, Design Automation, and Test Techniques. <i>IEEE Transactions on Biomedical Circuits and Systems</i> , <b>2019</b> , 13, 292-313	5.1	19
551	CAD-Base. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2019</b> , 24, 1-30	1.5	18
550	Layout-Aware Mixture Preparation of Biochemical Fluids on Application-Specific Digital Microfluidic Biochips. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2015</b> , 20, 1-34	1.5	18
549	. <i>IEEE Design and Test</i> , <b>2015</b> , 32, 8-19	1.4	18
548	Advances in Design Automation Techniques for Digital-Microfluidic Biochips <b>2015,</b> 190-223		18
547	Structural and Functional Test Methods for Micro-Electro-Dot-Array Digital Microfluidic Biochips. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2018</b> , 37, 968-981	2.5	18
546	Impact of Electrostatic Coupling and Wafer-Bonding Defects on Delay Testing of Monolithic 3D Integrated Circuits. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , <b>2017</b> , 13, 1-23	1.7	18
545	Experimental demonstration of error recovery in an integrated cyberphysical digital-microfluidic platform <b>2015,</b>		18

544	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2000</b> , 8, 633-636	2.6	18
543	Computation-oriented fault-tolerance schemes for RRAM computing systems <b>2017</b> ,		17
542	Execution of provably secure assays on MEDA biochips to thwart attacks <b>2019</b> ,		17
541	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2015</b> , 23, 317-330	2.6	17
540	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2016</b> , 35, 559-572	2.5	17
539	Test compaction for small-delay defects using an effective path selection scheme. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2013</b> , 18, 1-23	1.5	17
538	Reliability-Driven Pipelined Scan-Like Testing of Digital Microfluidic Biochips <b>2014</b> ,		17
537	Simultaneous Optimization of Droplet Routing and Control-Pin Mapping to Electrodes in Digital Microfluidic Biochips. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2012</b> , 31, 242-254	2.5	17
536	Crosstalk- and Process Variations-Aware High-Quality Tests for Small-Delay Defects. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2013</b> , 21, 1129-1142	2.6	17
535	<b>2010</b> ,		17
534	Test bus sizing for system-on-a-chip. <i>IEEE Transactions on Computers</i> , <b>2002</b> , 51, 449-459	2.5	17
533	Built-in self-test for micro-electrode-dot-array digital microfluidic biochips <b>2016</b> ,		17
532	Test Resource Partitioning for System-on-a-Chip. <i>Frontiers in Electronic Testing</i> , <b>2002</b> ,		17
531	. <i>IEEE Transactions on Multi-Scale Computing Systems</i> , <b>2018</b> , 4, 577-592		16
530	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2019</b> , 38, 589-603	2.5	16
529	Security Implications of Cyberphysical Flow-Based Microfluidic Biochips <b>2017</b> ,		16
528	Design automation and testing of monolithic 3D ICs: Opportunities, challenges, and solutions: (Invited paper) <b>2017</b> ,		16
527	Droplet Size-Aware and Error-Correcting Sample Preparation Using Micro-Electrode-Dot-Array Digital Microfluidic Biochips. <i>IEEE Transactions on Biomedical Circuits and Systems</i> , <b>2017</b> , 11, 1380-1391	5.1	16

526	Theory and analysis of generalized mixing and dilution of biochemical fluids using digital microfluidic biochips. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , <b>2014</b> , 11, 1-33	1.7	16
525	Fault recovery based on checkpointing for hard real-time embedded systems		16
524	Synthesis of Error-Recovery Protocols for Micro-Electrode-Dot-Array Digital Microfluidic Biochips. <i>Transactions on Embedded Computing Systems</i> , <b>2017</b> , 16, 1-22	1.8	15
523	Fault tolerance in neuromorphic computing systems <b>2019</b> ,		15
522	On Producing Linear Dilution Gradient of a Sample with a Digital Microfluidic Biochip <b>2013</b> ,		15
521	Knowledge discovery and knowledge transfer in board-level functional fault diagnosis <b>2014</b> ,		15
520	<b>2012</b> ,		15
519	Design of cyberphysical digital microfluidic biochips under completion-time uncertainties in fluidic operations <b>2013</b> ,		15
518	Integrated droplet routing in the synthesis of microfluidic biochips. <i>Proceedings - Design Automation Conference</i> , <b>2007</b> ,		15
517	Energy-aware deterministic fault tolerance in distributed real-time embedded systems <b>2004</b> ,		15
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328	Synthesis of a Cyberphysical Hybrid Microfluidic Platform for Single-Cell Analysis. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2019</b> , 38, 1237-1250	2.5	5
327	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2014</b> , 33, 903-916	2.5	5
326	Reproduction and Detection of Board-Level Functional Failure. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2012</b> , 31, 630-643	2.5	5
325	Routing-aware resource allocation for mixture preparation in digital microfluidic biochips <b>2013</b> ,		5
324	Error recovery in digital microfluidics for personalized medicine <b>2015</b> ,		5
323	Counter-Based Output Selection for Test Response Compaction. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2013</b> , 32, 152-164	2.5	5
322	Face-to-face bus design with built-in self-test in 3D ICs <b>2013</b> ,		5
321	Delay Test and Small-Delay Defects <b>2011</b> , 21-36		5
320	Soft error-aware design optimization of low power and time-constrained embedded systems <b>2010</b> ,		5
319	Digital Microfluidic Biochips: A Vision for Functional Diversity and More Than Moore <b>2010</b> ,		5
318	An Energy-Efficient Data Delivery Scheme for Delay-Sensitive Traffic in Wireless Sensor Networks. <i>International Journal of Distributed Sensor Networks</i> , <b>2010</b> , 6, 792068	1.7	5
317	Pin-Constrained Designs of Digital Microfluidic Biochips for High-Throughput Bioassays <b>2010</b> ,		5
316	Seed selection in LFSR-reseeding-based test compression for the detection of small-delay defects <b>2009</b> ,		5
315	Test generation for clock-domain crossing faults in integrated circuits <b>2012</b> ,		5
314	<b>2012</b> ,		5
313	Functional Test-Sequence Grading at Register-Transfer Level. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2012</b> , 20, 1890-1894	2.6	5
312	Optimization of Dual-Speed TAM Architectures for Efficient Modular Testing of SOCs. <i>IEEE Transactions on Computers</i> , <b>2007</b> , 56, 120-133	2.5	5
311	Balance testing and balance-testable design of logic circuits. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>1996</b> , 8, 71-86	0.7	5

310	Secure Assay Execution on MEDA Biochips to Thwart Attacks Using Real-Time Sensing. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2020</b> , 25, 1-25	1.5	5
309	Algorithmic Fault Detection for RRAM-based Matrix Operations. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2020</b> , 25, 1-31	1.5	5
308	On Concurrent Test of Core-Based SOC Design. <i>Frontiers in Electronic Testing</i> , <b>2002</b> , 37-50		5
307	Pre-bond testing of the silicon interposer in 2.5D ICs <b>2016</b> ,		5
306	Bio-chemical Assay Locking to Thwart Bio-IP Theft. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2020</b> , 25, 1-20	1.5	5
305	Advances in Design and Test of Monolithic 3-D ICs. <i>IEEE Design and Test</i> , <b>2020</b> , 37, 92-100	1.4	5
304	Acoustoelectronic nanotweezers enable dynamic and large-scale control of nanomaterials. <i>Nature Communications</i> , <b>2021</b> , 12, 3844	17.4	5
303	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2021</b> , 40, 143-156	2.5	5
302	Toward Hardware-Based IP Vulnerability Detection and Post-Deployment Patching in Systems-on-Chip. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2021</b> , 40, 1158-1171	2.5	5
301	Modeling Silicon-Photonic Neural Networks under Uncertainties <b>2021</b> ,		5
300	Built-In Self-Diagnosis and Fault-Tolerant Daisy-Chain Design in MEDA Biochips* <b>2018</b> ,		5
299	Robust TSV-based 3D NoC design to counteract electromigration and crosstalk noise <b>2017</b> ,		4
298	RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs <b>2019</b> ,		4
297	Synthesis of Reconfigurable Flow-Based Biochips for Scalable Single-Cell Screening. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2019</b> , 38, 2255-2270	2.5	4
296	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2015</b> , 34, 1873-1884	2.5	4
295	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2015</b> , 34, 122-135	2.5	4
294	Self-learning and adaptive board-level functional fault diagnosis <b>2015</b> ,		4
293	Jump test for metallic CNTs in CNFET-based SRAM <b>2015</b> ,		4

292	Reliability-Oriented IEEE Std. 1687 Network Design and Block-Aware High-Level Synthesis for MEDA Biochips* <b>2020</b> ,		4
291	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2020</b> , 39, 4908-4920	2.5	4
290	The hype, myths, and realities of testing 3D integrated circuits <b>2016</b> ,		4
289	Optimization of the IEEE 1687 access network for hybrid access schedules <b>2016</b> ,		4
288	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2016</b> , 35, 1192-1205	2.5	4
287	Securing JTAG against data-integrity attacks <b>2018</b> ,		4
286	Changepoint-Based Anomaly Detection for Prognostic Diagnosis in a Core Router System. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2019</b> , 38, 1331-1344	2.5	4
285	Generation of Effective 1-Detect TDF Patterns for Detecting Small-Delay Defects. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2013</b> , 32, 1583-1594	2.5	4
284	Handling Missing Syndromes in Board-Level Functional-Fault Diagnosis <b>2013</b> ,		4
283	<b>2017</b> ,		4
282	ExTest Scheduling and Optimization for 2.5-D SoCs With Wrapped Tiles. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2017</b> , 36, 1030-1042	2.5	4
281	Prebond Testing and Test-Path Design for the Silicon Interposer in 2.5-D ICs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2017</b> , 36, 1406-1419	2.5	4
280	Symbol-based health-status analysis in a core router system <b>2017</b> ,		4
279	Interconnect Testing and Test-Path Scheduling for Interposer-Based 2.5-D ICs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2015</b> , 34, 136-149	2.5	4
278	On-Line Error Detection in Digital Microfluidic Biochips <b>2012</b> ,		4
277	Generation of Compact Stuck-At Test Sets Targeting Unmodeled Defects. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2011</b> , 30, 787-791	2.5	4
276	Testing of Low-Cost Digital Microfluidic Biochips with Non-regular Array Layouts <b>2010</b> ,		4
275	A Noise-Aware Hybrid Method for SDD Pattern Grading and Selection <b>2010</b> ,		4



274	A BIST scheme for testing and repair of multi-mode power switches <b>2011</b> ,		4
273	<b>2009</b> ,		4
272	SOC test-architecture optimization for the testing of embedded cores and signal-integrity faults on core-external interconnects. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2009</b> , 14, 1-27	1.5	4
271	Digital microfluidic biochips <b>2011</b> ,		4
270	Connecting fabrication defects to fault models and simulation program with integrated circuit emphasis simulations for DNA self-assembled nanoelectronics. <i>IET Computers and Digital Techniques</i> , <b>2009</b> , 3, 553	0.9	4
269	Power-aware SoC test planning for effective utilization of port-scalable testers. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2008</b> , 13, 1-19	1.5	4
268	Built-in Self-test and Defect Tolerance in Molecular Electronics-based Nanofabrics. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>2007</b> , 23, 145-161	0.7	4
267	Runtime Identification of Hardware Trojans by Feature Analysis on Gate-Level Unstructured Data and Anomaly Detection. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2020</b> , 25, 1-23	1.5	4
266	Sensor-Array Optimization Based on Time-Series Data Analytics for Sanitation-Related Malodor Detection. <i>IEEE Transactions on Biomedical Circuits and Systems</i> , <b>2020</b> , 14, 705-714	5.1	4
265	Hardware Design and Fault-Tolerant Synthesis for Digital Acoustofluidic Biochips. <i>IEEE Transactions on Biomedical Circuits and Systems</i> , <b>2020</b> , 14, 1065-1078	5.1	4
264	Knowledge Transfer in Board-Level Functional Fault Identification using Domain Adaptation <b>2019</b> ,		4
263	Synthesis of Tamper-Resistant Pin-Constrained Digital Microfluidic Biochips. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2020</b> , 39, 171-184	2.5	4
262	C-Testing and Efficient Fault Localization for AI Accelerators*. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2021</b> , 1-1	2.5	4
261	Variation-Aware Delay Fault Testing for Carbon-Nanotube FET Circuits. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2021</b> , 29, 409-422	2.6	4
260	Access-Time Minimization in the IEEE 1687 Network Using Broadcast and Hardware Parallelism <b>2018</b> ,		4
259	Abetting Planned Obsolescence by Aging 3D Networks-on-Chip <b>2018</b> ,		4
258	An Integrated Framework for the Design and Optimization of SOC Test Solutions. <i>Frontiers in Electronic Testing</i> , <b>2002</b> , 21-36		4
257	Tackling Test Challenges for Interposer-Based 2.5-D Integrated Circuits. <i>IEEE Design and Test</i> , <b>2017</b> , 34, 72-79	1.4	3

256	Reliable Power Delivery and Analysis of Power-Supply Noise During Testing in Monolithic 3D ICs <b>2019,</b>		3
255	Security Assessment of Microfluidic Immunoassays <b>2019,</b>		3
254	Data-Driven Optimization of Order Admission Policies in a Digital Print Factory. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2015</b> , 20, 1-25	1.5	3
253	ExTest scheduling for 2.5D system-on-chip integrated circuits <b>2015,</b>		3
252	GRAMARCH: A GPU-ReRAM based Heterogeneous Architecture for Neural Image Segmentation <b>2020,</b>		3
251	<b>2020,</b>		3
250	Exact Synthesis of Biomolecular Protocols for Multiple Sample Pathways on Digital Microfluidic Biochips <b>2018,</b>		3
249	Workload-Aware Static Aging Monitoring and Mitigation of Timing-Critical Flip-Flops. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2018</b> , 37, 2098-2110	2.5	3
248	Online Soft-Error Vulnerability Estimation for Memory Arrays and Logic Cores. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2018</b> , 37, 499-511	2.5	3
247	A design-for-test solution for monolithic 3D integrated circuits <b>2016,</b>		3
246	Online soft-error vulnerability estimation for memory arrays <b>2016,</b>		3
245	An inter-layer interconnect BIST solution for monolithic 3D ICs <b>2018,</b>		3
244	Test and Design-for-Testability Solutions for 3D Integrated Circuits. <i>IPSJ Transactions on System LSI Design Methodology</i> , <b>2014</b> , 7, 56-73	0.2	3
243	Software-based online self-testing of network-on-chip using bounded model checking <b>2017,</b>		3
242	Sortex: Efficient timing-driven synthesis of reconfigurable flow-based biochips for scalable single-cell screening <b>2017,</b>		3
241	<b>2015,</b>		3
240	Test-access-mechanism optimization for multi-Vdd SoCs <b>2015,</b>		3
239	Demand-driven mixture preparation and droplet streaming using digital microfluidic biochips <b>2014,</b>		3

238	Demand-Driven Mixture Preparation and Droplet Streaming using Digital Microfluidic Biochips <b>2014,</b>		3
237	Automated path planning for washing in digital microfluidic biochips <b>2012,</b>		3
236	<b>2013,</b>		3
235	MVP: Minimum-Violations Partitioning for Reducing Capture Power in At-Speed Delay-Fault Testing. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2011</b> , 30, 1762-1767	2.5	3
234	Fault Diagnosis in Lab-on-Chip Using Digital Microfluidic Logic Gates. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>2011</b> , 27, 69-83	0.7	3
233	Datacollection in Event-Driven Wireless Sensor Networks with Mobile Sinks. <i>International Journal of Distributed Sensor Networks</i> , <b>2010</b> , 6, 402680	1.7	3
232	Signature Analysis for Testing, Diagnosis, and Repair of Multi-mode Power Switches <b>2011,</b>		3
231	Ranking of Suspect Faulty Blocks Using Dataflow Analysis and Dempster-Shafer Theory for the Diagnosis of Board-Level Functional Failures <b>2011,</b>		3
230	Pre-bond testing of die logic and TSVs in high performance 3D-SICs <b>2012,</b>		3
229	Wafer-Level Defect Screening for Big-D/Small-AIMixed-Signal SoCs. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2009</b> , 17, 587-592	2.6	3
228	Power Management Using Test-Pattern Ordering for Wafer-Level Test During Burn-In. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2009</b> , 17, 1730-1741	2.6	3
227	Wafer-Level Modular Testing of Core-Based SoCs. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2007</b> , 15, 1144-1154	2.6	3
226	An ECO Technique for Removing Crosstalk Violations in Clock Networks <b>2007,</b>		3
225	Design and analysis of compact dictionaries for diagnosis in scan-BIST. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2005</b> , 13, 979-984	2.6	3
224	Space compaction of test responses using orthogonal transmission functions [logic testing]. <i>IEEE Transactions on Instrumentation and Measurement</i> , <b>2003</b> , 52, 1353-1362	5.2	3
223	Pruning-based energy-optimal device scheduling for hard real-time systems <b>2002,</b>		3
222	Unsupervised Root-Cause Analysis for Integrated Systems <b>2020,</b>		3
221	C-Testing of AI Accelerators * <b>2020,</b>		3

220	Offline Washing Schemes for Residue Removal in Digital Microfluidic Biochips. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2015</b> , 21, 1-33	1.5	3
219	Microelectrofluidic Systems <b>2002</b> ,		3
218	Test Generation for Flow-Based Microfluidic Biochips With General Architectures. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2020</b> , 39, 2530-2543	2.5	3
217	Adaptation of Biochemical Protocols to Handle Technology-Change for Digital Microfluidics. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2016</b> , 1-1	2.5	3
216	Sensor-Array Optimization Based on Mutual Information for Sanitation-Related Malodor Alerts <b>2019</b> ,		3
215	Fault-Tolerant Neuromorphic Computing Systems <b>2019</b> ,		3
214	On Designing Efficient and Reliable Nonvolatile Memory-Based Computing-In-Memory Accelerators <b>2019</b> ,		3
213	Hardware Fault Tolerance for Binary RRAM Crossbars <b>2019</b> ,		3
212	Programmable Daisy chaining of Microelectrodes for IP Protection in MEDA Biochips <b>2019</b> ,		3
211	An Interlayer Interconnect BIST and Diagnosis Solution for Monolithic 3-D ICs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2020</b> , 39, 3056-3066	2.5	3
210	Board-Level Functional Fault Identification Using Streaming Data. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2021</b> , 40, 1920-1933	2.5	3
209	Fault Modeling and Efficient Testing of Memristor-Based Memory. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , <b>2021</b> , 1-12	3.9	3
208	ReGraphX: NoC-enabled 3D Heterogeneous ReRAM Architecture for Training Graph Neural Networks <b>2021</b> ,		3
207	Tamper-resistant pin-constrained digital microfluidic biochips <b>2018</b> ,		3
206	Design-for-testability for continuous-flow microfluidic biochips <b>2018</b> ,		3
205	On Designing All-Optical Multipliers Using Mach-Zender Interferometers <b>2018</b> ,		3
204	A Novel Reconfigurable Wrapper for Testing of Embedded Core-Based SOCs and its Associated Scheduling Algorithm. <i>Frontiers in Electronic Testing</i> , <b>2002</b> , 51-70		3
203	Test and Design-for-Testability Solutions for Monolithic 3D Integrated Circuits <b>2019</b> ,		2

202	<b>2020,</b>		2
201	Testing 3D-SoCs Using 2-D Time-Division Multiplexing. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2018</b> , 37, 3177-3185	2.5	2
200	Two-dimensional time-division multiplexing for 3D-SoCs <b>2016,</b>		2
199	A Distributed, Reconfigurable, and Reusable BIST Infrastructure for Test and Diagnosis of 3-D-Stacked ICs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2016</b> , 35, 309-322	2.5	2
198	Demand-Driven Single- and Multitarget Mixture Preparation Using Digital Microfluidic Biochips. <i>ACM Transactions on Design Automation of Electronic Systems</i> , <b>2018</b> , 23, 1-26	1.5	2
197	Can Multi-Layer Microfluidic Design Methods Aid Bio-Intellectual Property Protection? <b>2019,</b>		2
196	Retiming for Delay Recovery After DfT Insertion on Interdie Paths in 3-D ICs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2014</b> , 33, 464-475	2.5	2
195	Post-DfT-insertion retiming for delay recovery on inter-die paths in 3D ICs <b>2013,</b>		2
194	Robust optimization of test-architecture designs for core-based SoCs <b>2013,</b>		2
193	Testing of flow-based microfluidic biochips <b>2013,</b>		2
192	Knowledge-Driven Board-Level Functional Fault Diagnosis <b>2017,</b>		2
191	<b>2015,</b>		2
190	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2015</b> , 23, 1-17	2.6	2
189	Cyber-physical integration in programmable microfluidic biochips <b>2015,</b>		2
188	Efficient LFSR Reseeding Based on Internal-Response Feedback. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>2014</b> , 30, 673-685	0.7	2
187	Optimization of heaters in a digital microfluidic biochip for the polymerase chain reaction <b>2014,</b>		2
186	Reduced-Complexity Transition-Fault Test Generation for Non-scan Circuits through High-Level Mutant Injection <b>2012,</b>		2
185	Testing of Low-cost Digital Microfluidic Biochips with Non-Regular Array Layouts. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>2012</b> , 28, 243-255	0.7	2

184	A New LFSR Reseeding Scheme via Internal Response Feedback <b>2013</b> ,		2
183	A Metric to Target Small-Delay Defects in Industrial Circuits. <i>IEEE Design and Test of Computers</i> , <b>2011</b> , 28, 52-61		2
182	Defect Coverage-Driven Window-Based Test Compression <b>2010</b> ,		2
181	Mimicking of Functional State Space with Structural Tests for the Diagnosis of Board-Level Functional Failures <b>2010</b> ,		2
180	Toward fault-tolerant and reconfigurable digital microfluidic biochips <b>2010</b> ,		2
179	3D-Scalable Adaptive Scan (3D-SAS) <b>2012</b> ,		2
178	RTL DFT techniques to enhance defect coverage for functional test sequences <b>2009</b> ,		2
177	Optimization of droplet routing for an n-plex bioassay on a digital microfluidic lab-on-chip <b>2009</b> ,		2
176	RTL DFT Techniques to Enhance Defect Coverage for Functional Test Sequences. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>2010</b> , 26, 151-164	0.7	2
175	Accelerated Functional Testing of Digital Microfluidic Biochips <b>2008</b> ,		2
174	Fabrication Defects and Fault Models for DNA Self-Assembled Nanoelectronics <b>2008</b> ,		2
173	Power Management for Wafer-Level Test During Burn-In <b>2008</b> ,		2
172	Guest Editors' Introduction: Biochips and Integrated Biosensor Platforms. <i>IEEE Design and Test of Computers</i> , <b>2007</b> , 24, 8-9		2
171	A Signature Analysis Technique for the Identification of Failing Vectors with Application to Scan-BIST*. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , <b>2004</b> , 20, 611-622	0.7	2
170	An Optimal Two-Mixer Dilution Engine with Digital Microfluidics for Low-Power Applications. <i>Journal of Low Power Electronics</i> , <b>2014</b> , 10, 506-518	1.2	2
169	CAS-BUS: A Test Access Mechanism and a Toolbox Environment for Core-Based System Chip Testing. <i>Frontiers in Electronic Testing</i> , <b>2002</b> , 91-109		2
168	On-Chip Dilution from Multiple Concentrations of a Sample Fluid Using Digital Microfluidics. <i>Communications in Computer and Information Science</i> , <b>2013</b> , 274-283	0.3	2
167	Multicast Test Architecture and Test Scheduling for Interposer-Based 2.5D ICs <b>2016</b> ,		2

166	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2020</b> , 39, 3531-3543	2.5	2
165	Digital-Microfluidic Biochips. <i>Computer</i> , <b>2016</b> , 49, 8-9	1.6	2
164	<b>2016</b> ,		2
163	A unified test and fault-tolerant multicast solution for network-on-chip designs <b>2016</b> ,		2
162	Fault Recovery in Micro-Electro-Dot-Array Digital Microfluidic Biochips Using an IJTAG NetworkBehaviors <b>2019</b> ,		2
161	Software-Based Self-Testing Using Bounded Model Checking for Out-of-Order Superscalar Processors. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2020</b> , 39, 714-727	2.5	2
160	Cyberphysical Microfluidic Biochips <b>2020</b> , 1-17		2
159	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2020</b> , 39, 4921-4934	2.5	2
158	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2021</b> , 40, 386-399	2.5	2
157	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2021</b> , 40, 1301-1314	2.5	2
156	Knowledge Transfer in Board-Level Functional Fault Diagnosis Enabled by Domain Adaptation. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2021</b> , 1-1	2.5	2
155	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2021</b> , 1-1	2.5	2
154	Efficient Identification of Critical Faults in Memristor Crossbars for Deep Neural Networks <b>2021</b> ,		2
153	Failure prediction based on anomaly detection for complex core routers <b>2018</b> ,		2
152	Learning to Train CNNs on Faulty ReRAM-based Manycore Accelerators. <i>Transactions on Embedded Computing Systems</i> , <b>2021</b> , 20, 1-23	1.8	2
151	. <i>IEEE Transactions on Information Forensics and Security</i> , <b>2021</b> , 16, 2076-2089	8	2
150	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2021</b> , 1-1	2.5	2
149	A Branch-&Bound Test-Access-Mechanism Optimization Method for Multi- $\mathbb{D}$ SoCs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2017</b> , 36, 1911-1924	2.5	1

148	Quo Vadis Test? The Past, the Present, and the Future: No Longer a Necessary Evil. <i>IEEE Design and Test</i> , <b>2017</b> , 34, 93-95	1.4	1
147	Testing of Interposer-Based 2.5D Integrated Circuits <b>2017</b> ,		1
146	Synterface. <i>Transactions on Embedded Computing Systems</i> , <b>2019</b> , 18, 1-21	1.8	1
145	Black-Box Test-Coverage Analysis and Test-Cost Reduction Based on a Bayesian Network Model <b>2019</b> ,		1
144	Anomaly Detection and Health-Status Analysis in a Core Router System. <i>IEEE Design and Test</i> , <b>2019</b> , 36, 7-17	1.4	1
143	Machine Learning-Based Aging Analysis <b>2019</b> , 265-289		1
142	Data-Driven Optimization and Knowledge Discovery for an Enterprise Information System <b>2015</b> ,		1
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