Bijan Alizadeh

List of Publications by Year in Descending Order

63 papers	322 citations	9 h-index	14 g-index
82 ext. papers	445 ext. citations	2.4 avg, IF	4.16 L-index

#	Paper	IF	Citations
63	Hardware Patching Methodology for Neutralizing Timing Hardware Trojans Using Vulnerability Analysis and Time Borrowing Scheme. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2022**, 1-1	3.5	0
62	Enhancing Hardware Trojan Detection Sensitivity Using Partition-Based Shuffling Scheme. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 266-270	3.5	3
61	SAT-Based Integrated Hardware Trojan Detection and Localization Approach Through Path-Delay Analysis. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 2850-2854	3.5	2
60	PODEM: A low-cost property-based design modification for detecting Hardware Trojans in resource-constraint IoT devices. *Journal of Network and Computer Applications*, **2020**, 167, 102713	7.9	3
59	Incremental SAT-Based Correction of Gate Level Circuits by Reusing Partially Corrected Circuits. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 3063-3067	3.5	2
58	Combinational Hybrid Signal Selection With Updated Reachability Lists for Post-Silicon Debug. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 272-276	2.5	
57	PMTP: A MAX-SAT-Based Approach to Detect Hardware Trojan Using Propagation of Maximum Transition Probability. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 25-33	2.5	10
56	FPGA-Based Implementation of a Real-Time Object Recognition System Using Convolutional Neural Network. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 755-759	3.5	10
55	. *IEEE Transactions on Instrumentation and Measurement*, **2019**, 68, 4326-4334	5.2	4
54	A Dynamic Timing Error Avoidance Technique Using Prediction Logic in High-Performance Designs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 734-737	2.6	0
53	Data-path aware high-level ECO synthesis. *The Integration VLSI Journal*, **2019**, 65, 88-96	1.4	
52	Incremental SAT-Based Accurate Auto-Correction of Sequential Circuits Through Automatic Test Pattern Generation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 245-252	2.5	5
51	FPGA-Based Implementation of a Novel Method for Estimating the Brillouin Frequency Shift in BOTDA and BOTDR Sensors. *IEEE Sensors Journal*, **2018**, 18, 2015-2022	4	11
50	Automatic Correction of Dynamic Power Management Architecture in Modern Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 308-318	2.6	1
49	QBF-Based Post-Silicon Debug of Speed-Paths Under Timing Variations. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 4326-4335	3.9	1
48	Scalable Symbolic Simulation-Based Automatic Correction of Modern Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 1845-1853	2.6	
47	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 198-209	2.6	3

46	Improved Range Analysis in Fixed-Point Polynomial Data-Path. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1925-1929	2.5	4
45	A Resource-Limited Hardware Accelerator for Convolutional Neural Networks in Embedded Vision Applications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 1217-1221	3.5	37
44	Bridging Presilicon and Postsilicon Debugging by Instruction-Based Trace Signal Selection in Modern Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2059-2070	2.6	2
43	Scalable SMT-Based Equivalence Checking of Nested Loop Pipelining in Behavioral Synthesis. *ACM Transactions on Design Automation of Electronic Systems*, **2017**, 22, 1-22	1.5	1
42	Reducing Search Space for Fault Diagnosis: A Probability-Based Scoring Approach **2017**,		3
41	Systematic Design Space Exploration of Floating-Point Expressions on FPGA. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 274-278	3.5	
40	A Hybrid Time Borrowing Technique to Improve the Performance of Digital Circuits in the Presence of Variations. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2017**, 64, 100-110	3.9	6
39	Genetic-Algorithm-Based FPGA Architectural Exploration Using Analytical Models. *ACM Transactions on Design Automation of Electronic Systems*, **2016**, 22, 1-17	1.5	0
38	A dynamic specification to automatically debug and correct various divider circuits. *The Integration VLSI Journal*, **2016**, 53, 100-114	1.4	1
37	Formally analyzing fault tolerance in datapath designs using equivalence checking **2016**,		2
36	UAFEA: Unified Analytical Framework for IA/AA-Based Error Analysis of Fixed-Point Polynomial Specifications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2016**, 63, 994-998	3.5	3
35	Low power scheduling in high-level synthesis using dual-Vth library **2015**,		2
34	Groebner basis based formal verification of large arithmetic circuits using Gaussian elimination and cone-based polynomial extraction. *Microprocessors and Microsystems*, **2015**, 39, 83-96	2.4	22
33	Analytical performance model for FPGA-based reconfigurable computing. *Microprocessors and Microsystems*, **2015**, 39, 796-806	2.4	8
32	UPF-based formal verification of low power techniques in modern processors **2015**,		3
31	Signature oriented model pruning to facilitate multi-threaded processors debugging **2015**,		2
30	A Timing Error Mitigation Technique for High Performance Designs **2015**,		5
29	Multi-objective Optimization of Floating Point Arithmetic Expressions Using Iterative Factorization **2015**,		3

28	In-Circuit Mutation-Based Automatic Correction of Certain Design Errors Using SAT Mechanisms **2015**,		9
27	Dynamic Flip-Flop Conversion: A Time-Borrowing Method for Performance Improvement of Low-Power Digital Circuits Prone to Variations. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 2724-2727	2.6	15
26	Automatic correction of certain design errors using mutation technique **2014**,		5
25	A Low-Power Enhanced Bitmask-Dictionary Scheme for Test Data Compression **2014**,		2
24	Improving polynomial datapath debugging with HEDs **2014**,		2
23	An analytical dynamic and leakage power model for FPGAs **2014**,		1
22	Automatic High-level Data-flow Synthesis and Optimization of Polynomial Datapaths Using Functional Decomposition. *IEEE Transactions on Computers*, **2014**, 1-1	2.5	4
21	Automated formal approach for debugging dividers using dynamic specification **2014**,		3
20	Effective Combination of Algebraic Techniques and Decision Diagrams to Formally Verify Large Arithmetic Circuits **2014**,		6
19	A Scalable Formal Debugging Approach with Auto-Correction Capability Based on Static Slicing and Dynamic Ranking for RTL Datapath Designs. *IEEE Transactions on Computers*, **2014**, 1-1	2.5	7
18	Formal equivalence verification and debugging techniques with auto-correction mechanism for RTL designs. *Microprocessors and Microsystems*, **2013**, 37, 1108-1121	2.4	10
17	A probabilistic approach for counterexample generation to aid design debugging **2013**,		3
16	A New Approach for Automatic Test Pattern Generation in Register Transfer Level Circuits. *IEEE Design and Test*, **2013**, 30, 49-59	1.4	4
15	A formal approach to debug polynomial datapath designs **2012**,		9
14	Formal Verification and Debugging of Precise Interrupts on High Performance Microprocessors. *ACM Transactions on Design Automation of Electronic Systems*, **2012**, 17, 1-8	1.5	6
13	Debugging and optimizing high performance superscalar out-of-order processors using formal verification techniques **2011**,		2
12	Coverage Driven High-Level Test Generation Using a Polynomial Model of Sequential Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 737-748	2.5	2
11	Pipelined Microprocessors Optimization and Debugging. *Lecture Notes in Computer Science*, **2010**, 435-444	0.9	1

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10	A debugging method for repairing post-silicon bugs of high performance processors in the fields **2010**,		3
9	Polynomial datapath optimization using constraint solving and formal modelling **2010**,		2
8	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1422-1435	2.5	18
7	Guided gate-level ATPG for sequential circuits using a high-level test generation approach **2010**,		5
6	A Formal Approach for Debugging Arithmetic Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2009**, 28, 742-754	2.5	18
5	A Unified Framework for Equivalence Verification of Datapath Oriented Applications. *IEICE Transactions on Information and Systems*, **2009**, E92-D, 985-994	0.6	6
4	Improved heuristics for finite word-length polynomial datapath optimization **2009**,		4
3	Sequential Equivalence Checking Using a Hybrid Boolean-Word Level Decision Diagram. *Communications in Computer and Information Science*, **2008**, 697-704	0.3	
2	Automatic Merge-Point Detection for Sequential Equivalence Checking of System-Level and RTL Descriptions **2007**, 129-144		6
1	A novel formal approach to generate high-level test vectors without ILP and SAT solvers **2007**,		3