Saeed Safari

List of Publications by Citations

66 papers	431 citations	10 h-index	17 g-index
83 ext. papers	572 ext. citations	1.9 avg, IF	3.68 L-index

#	Paper	IF	Citations
66	OPLE. *Transactions on Embedded Computing Systems*, **2015**, 14, 1-23	1.8	60
65	Yield and Speedup Improvements in Extensible Processors by Allocating Extra Cycles to Some Custom Instructions. *ACM Transactions on Design Automation of Electronic Systems*, **2016**, 21, 1-25	1.5	31
64	FPGA implementation of a biological neural network based on the Hodgkin-Huxley neuron model. *Frontiers in Neuroscience*, **2014**, 8, 379	5.1	27
63	Parallel scalable hardware implementation of asynchronous discrete particle swarm optimization. *Engineering Applications of Artificial Intelligence*, **2010**, 23, 177-187	7.2	22
62	Reliability in Application Specific Mesh-Based NoC Architectures **2008**,		19
61	Evaluation of SiC power devices for a high power density matrix converter **2012**,		16
60	Negative Exponential Distribution Traffic Pattern for Power/Performance Analysis of Network on Chips **2009**,		16
59	An efficient medium access control protocol for WSN-UAV. *Ad Hoc Networks*, **2016**, 52, 146-159	4.8	14
58	SEERAD: A high speed yet energy-efficient rounding-based approximate divider **2016**,		14
57	Time-domain modeling of nonlinear circuits using deep recurrent neural network technique. *AEU - International Journal of Electronics and Communications*, **2019**, 100, 66-74	2.8	11
56	Securing Embedded Processors against Power Analysis Based Side Channel Attacks Using Reconfigurable Architecture **2011**,		10
55	Fault Tolerant Arithmetic Operations with Multiple Error Detection and Correction **2007**,		9
54	SOPC-Based Architecture for Discrete Particle Swarm Optimization **2007**,		9
53	HW/SW architecture for soft-error cancellation in real-time operating system. *IEICE Electronics Express*, **2007**, 4, 755-761	0.5	9
52	A Scalable FPGA Architecture for Randomly Connected Networks of Hodgkin-Huxley Neurons. *Frontiers in Neuroscience*, **2018**, 12, 698	5.1	9
51	Dynamic behavioral modeling of nonlinear circuits using a novel recurrent neural network technique. *International Journal of Circuit Theory and Applications*, **2019**, 47, 1071-1085	2	8
50	A cross-layer SER analysis in the presence of PVTA variations. *Microelectronics Reliability*, **2015**, 55, 1013-1027	1.2	8

49	Designing an ultra-high-speed multiply-accumulate structure. *Microelectronics Journal*, **2008**, 39, 1476-1484	1.1	8
48	Reliability-Aware Task Scheduling using Clustered Replication for Multi-core Real-Time systems **2016**,		6
47	Fault-aware and Reconfigurable Routing Algorithms for Networks-on-Chip. *IETE Journal of Research* , **2011**, 57, 215	0.9	6
46	Scalable Architecture for on-Chip Neural Network Training using Swarm Intelligence **2008**,		6
45	A HW/SW Architecture to Reduce the Effects of Soft-Errors in Real-Time Operating System Services **2007**,		6
44	A cross-layer approach to online adaptive reliability prediction of transient faults **2015**,		5
43	Fast and accurate architectural vulnerability analysis for embedded processors using Instruction Vulnerability Factor. *Microprocessors and Microsystems*, **2016**, 42, 113-126	2.4	5
42	Fast implementation of dense stereo vision algorithms on a highly parallel SIMD architecture. *Journal of Real-Time Image Processing*, **2013**, 8, 421-435	1.9	5
41	The impact of switching frequency on input filter design for high power density matrix converter **2014**,		5
40	An efficient reliability simulation flow for evaluating the hot carrier injection effect in CMOS VLSI circuits **2012**,		5
39	Forecasting-Based Dynamic Virtual Channels Allocation for Power Optimization of Network-on-Chips **2009**,		5
38	Scalable architecture for on-chip neural network training using swarm intelligence **2008**,		5
37	HW/SW partitioning using discrete particle swarm **2007**,		5
36	Reliability aware throughput management of chip multi-processor architecture via thread migration. *Journal of Supercomputing*, **2016**, 72, 1363-1380	2.5	4
35	FPGA Implementation of a Cortical Network Based on the Hodgkin-Huxley Neuron Model. *Lecture Notes in Computer Science*, **2012**, 243-250	0.9	4
34	Highly parallel and fast implementation of stereo vision algorithms on MIMD many-core Tilera architecture **2012**,		4
33	An Intelligent MLFQ Scheduling Algorithm (IMLFQ) with Fault Tolerant Mechanism **2006**,		4
32	CMV: Clustered Majority Voting Reliability-Aware Task Scheduling for Multicore Real-Time Systems. *IEEE Transactions on Reliability*, **2019**, 68, 187-200	4.6	4

31	LORAP: Low-Overhead Power and Reliability-Aware Task Mapping Based on Instruction Footprint for Real-Time Applications **2017**,		3
30	Reliability-aware simultaneous multithreaded architecture using online architectural vulnerability factor estimation. *IET Computers and Digital Techniques*, **2015**, 9, 124-133	0.9	3
29	Reliability assessment of networks-on-chip based on analytical models. *Journal of Zhejiang University: Science A*, **2009**, 10, 1801-1814	2.1	3
28	Real-Time Parallel Implementation of SSD Stereo Vision Algorithm on CSX SIMD Architecture. *Lecture Notes in Computer Science*, **2009**, 808-818	0.9	3
27	Cross-layer custom instruction selection to address PVTA variations and soft error. *Microelectronics Reliability*, **2015**, 55, 2423-2438	1.2	2
26	Design of NBTI-resilient extensible processors. *The Integration VLSI Journal*, **2015**, 49, 22-34	1.4	2
25	Considering the effect of process variations during the ISA extension design flow. *Microprocessors and Microsystems*, **2013**, 37, 713-724	2.4	2
24	An instance-based SER analysis in the presence of PVTA variations **2014**,		2
23	Analysis of single-event effects in embedded processors for non-uniform fault tolerant design **2009** ,		2
22	On-Chip Verification of NoCs Using Assertion Processors **2007**,		2
21	Improving Robustness of Real-Time Operating Systems (RTOS) Services Related to Soft-Errors **2007** ,		2
20	A Novel Merged Multiplier-Accumulator Embedded in DSP Coprocessor **2006**,		2
19	A reconfigurable real-time neuromorphic hardware for spiking winner-take-all network. *International Journal of Circuit Theory and Applications*, **2020**, 48, 2141-2152	2	2
18	PVTA-aware approximate custom instruction extension technique: A cross-layer approach. *Microelectronics Reliability*, **2016**, 63, 267-277	1.2	1
17	A Majority-Based Reliability-Aware Task-Mapping in High-Performance Homogenous NoC Architectures **2016**,		1
16	Impact of Process Variations on Speedup and Maximum Achievable Frequency of Extensible Processors. *ACM Journal on Emerging Technologies in Computing Systems*, **2014**, 10, 1-25	1.7	1
15	**2012**,		1
14	Evaluation of normally-off SiC JFET for a high power density matrix converter **2012**,		1

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13	Comparative performance evaluation of SiC power devices for high temperature and high frequency matrix converter **2013**,		1
12	A 65nm 10GHz pipelined MAC structure **2008**,		1
11	Mesh architecture for hardware implementation of Particle Swarm Optimization **2007**,		1
10	15GHz low-voltage-swing carry-lookahead adder. *IEICE Electronics Express*, **2007**, 4, 696-700	0.5	1
9	A parameterized graph-based framework for high-level test synthesis. *The Integration VLSI Journal*, **2006**, 39, 363-381	1.4	1
8	Fast Parallel Model Estimation on the Cell Broadband Engine. *Lecture Notes in Computer Science*, **2010**, 469-480	0.9	1
7	Statistical analysis of asynchronous pipelines in presence of process variation using formal models. *The Integration VLSI Journal*, **2016**, 55, 98-117	1.4	1
6	Implementation-aware selection of the custom instruction set for extensible processors. *Microprocessors and Microsystems*, **2014**, 38, 681-691	2.4	0
5	Modeling Soft Error Propagation in Near-Threshold Combinational Circuits Using Neural Networks. *Journal of Electronic Testing: Theory and Applications (JETTA)*, **2019**, 35, 401-412	0.7	
4	Fast and accurate FPGA-based framework for processor architecture vulnerability analysis. *The Integration VLSI Journal*, **2016**, 53, 14-26	1.4	
3	An efficient temperature dependent hot carrier injection reliability simulation flow. *Microelectronics Reliability*, **2016**, 57, 10-19	1.2	
2	A memory-efficient canonical data structure for decimal floating point arithmetic systems modeling and verification. *Turkish Journal of Electrical Engineering and Computer Sciences*, **2019**, 27, 471-483	0.9	
1	A multiple-event propagation model in near-threshold combinational circuits using neural networks. *Journal of Computational Electronics*, **2021**, 20, 1032-1042	1.8	