Piet Wambacq

List of Publications by Year
in descending order

90 papers	3,057 citations	196777 29 h-index	198040 52 g-index
90 all docs	90 docs citations	90 times ranked	2426 citing authors

#	Article	IF	Citations
1	Design and Analysis of a 140-GHz T/R Front-End Module in 22-nm FD-SOI CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 1300-1313.	3.5	8
2	A D-Band Low-Power and High-Efficiency Frequency Multiply-by-9 FMCW Radar Transmitter in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 2114-2129.	3.5	10
3	A 950 MHz Clock 47.5 MHz BW 4.7 mW 67 dB SNDR Discrete Time Delta Sigma ADC Leveraging Ring Amplification and Split-Source Comparator Based Quantizer in 28 nm CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 2068-2077.	3.5	5
4	A Stacked Segmented Adaptive Power Amplifier in 22nm FD-SOI. IEEE Microwave and Wireless Components Letters, 2022, 32, 983-986.	2.0	1
5	A 67-mW D-Band FMCW I/Q Radar Receiver With an N-Path Spillover Notch Filter in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 1982-1996.	3.5	5
6	Design and Analysis of 55â€“63-GHz Fundamental Quad-Core VCO With NMOS-Only Stacked Oscillator in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 1997-2010.	3.5	10
7	Linearity Assessment of GaN HEMTs on Si using Nonlinear Characterisation. , 2022, , .		1
8	A Low-Power Reflection-Coefficient Sensor for 28-GHz Beamforming Transmitters in 22-nm FD-SOI CMOS. IEEE Journal of Solid-State Circuits, 2021, 56, 3704-3714.	3.5	5
9	Design and Analysis of a 28 GHz T/R Front-End Module in 22-nm FD-SOI CMOS Technology. IEEE Transactions on Microwave Theory and Techniques, 2021, 69, 2841-2853.	2.9	12
10	A 12 Bit 4.7-MS/s 260.5-Î¼W Digital Feed-Forward Incremental-Î£Î”-SAR ADC in 0.13-Î¼m CMOS for Image Sensors. IEEE Sensors Journal, 2021, 21, 21653-21666.	2.4	3
11	A Wideband 62-mW 60-GHz FMCW Radar in 28-nm CMOS. IEEE Transactions on Microwave Theory and Techniques, 2021, 69, 2921-2935.	2.9	18
12	A 140 GHz T/R Front-End Module in 22 nm FD-SOI CMOS. , 2021, , .		12
13	A 135-155 GHz 9.7%/16.6% DC-RF/DC-EIRP Efficiency Frequency Multiply-by-9 FMCW Transmitter in 28 nm CMOS. , 2021, , .		7
14	A 28-GHz SOI-CMOS Doherty Power Amplifier With a Compact Transformer-Based Output Combiner. IEEE Transactions on Microwave Theory and Techniques, 2021, 69, 2795-2808.	2.9	35
15	A 28-nm-CMOS Based 145-GHz FMCW Radar: System, Circuits, and Characterization. IEEE Journal of Solid-State Circuits, 2021, 56, 1975-1993.	3.5	32
16	A 55â€“63 GHz fundamental Quad-Core VCO with NMOS-only stacked oscillator in 28 nm CMOS. , 2021, , .		1
17	A 67mW D-band FMCW I/Q Radar Receiver with an N-path Spillover Notch Filter in 28nm CMOS. , 2021, , .		1
18	Analysis of Gate-Metal Resistance in CMOS-Compatible RF GaN HEMTs. IEEE Transactions on Electron Devices, 2020, 67, 4592-4596.	1.6	7

#	Article	IF	Citations
19	A 12-mW 10-GHz FMCW PLL Based on an Integrating DAC With 28-kHz RMS-Frequency-Error for 23-MHz/Î¼s Slope and 1.2-GHz Chirp-Bandwidth. IEEE Journal of Solid-State Circuits, 2020, 55, 3294-3307.	3.5	13
20	A 28 GHz front-end module with T/R switch achieving 17.2 dBm P_{sat}, 21.5% PAE_{max} and 3.2 dB NF in 22 nm FD-SOI for 5G communication. , 2020, , .		7
21	An integrated 132-147GHz power source with +27dBm EIRP. , 2020, , .		6
22	(Invited) Advanced Transistors for High Frequency Applications. ECS Transactions, 2020, 97, 27-38.	0.3	2
23	Design of D-Band Transformer-Based Gain-Boosting Class-AB Power Amplifiers in Silicon Technologies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1447-1458.	3.5	19
24	Low 1/f³ Noise Corner LC-VCO Design Using Flicker Noise Filtering Technique in 22nm FD-SOI. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1469-1480.	3.5	12
25	Analysis of a 28-nm CMOS Fast-Lock Bang-Bang Digital PLL With 220-fs RMS Jitter for Millimeter-Wave Communication. IEEE Journal of Solid-State Circuits, 2020, 55, 1854-1863.	3.5	25
26	(Plenary) The Revival of Compound Semiconductors and How They Will Change the World in a 5G/6G Era. ECS Transactions, 2020, 98, 15-25.	0.3	4
27	A 5.5-GHz Background-Calibrated Subsampling Polar Transmitter With â^'41.3-dB EVM at 1024 QAM in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 1059-1073.	3.5	19
28	A 1-GS/s, 12-b, Single-Channel Pipelined ADC With Dead-Zone-Degenerated Ring Amplifiers. IEEE Journal of Solid-State Circuits, 2019, 54, 646-658.	3.5	40
29	9.4 A 145GHz FMCW-Radar Transceiver in 28nm CMOS. , 2019, , .		45
30	A 112-142GHz Power Amplifier with Regenerative Reactive Feedback achieving 17dBm peak P_{sat} at 13% PAE. , 2019, , .		11
31	A Single-Channel, 600-MS/s, 12-b, Ringamp-Based Pipelined ADC in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 403-416.	3.5	35
32	A 23 GHz Low-Phase-Noise Transformer-Feedback VCO in 22nm FD-SOI with a FOMT of 191dBc/Hz. , 2018, , .		6
33	Comparator hysteresis compensation for decision feedback equalisers. Electronics Letters, 2018, 54, 1421-1422.	0.5	1
34	Analysis and Design of a CMOS Ultra-High-Speed Burst Mode Imager with In-Situ Storage Topology Featuring In-Pixel CDS Amplification. Sensors, 2018, 18, 3683.	2.1	5
35	A 60-GHz 8-Way Phased-Array Front-End With T/R Switching and Calibration-Free Beamsteering in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 2001-2011.	3.5	23
36	Statistical Timing Analysis Considering Device and Interconnect Variability for BEOL Requirements in the 5-nm Node and Beyond. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1669-1680.	2.1	40

#	Article	IF	Citations
37	A 21-dBm I/Q Digital Transmitter Using Stacked Output Stage in 28-nm Bulk CMOS Technology. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 4744-4757.	2.9	10
38	A 79-GHz 2 $imes $ 2 MIMO PMCW Radar SoC in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2017, 52, 2613-2626.	3.5	110
39	Adaptive RF Front-Ends Using Electrical-Balance Duplexers and Tuned SAW Resonators. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 4621-4628.	2.9	36
40	A 54â€“64.8 GHz subharmonically injection-locked frequency synthesizer with transmitter EVM between â˜26.5 dB and â˜28.8 dB in 28 nm CMOS. , 2017, , .		6
41	A 79GHz 2Ã—2 MIMO PMCW radar SoC in 28nm CMOS. , 2016, , .		7
42	A +70-dBm IIP3 Electrical-Balance Duplexer for Highly Integrated Tunable Front-Ends. IEEE Transactions on Microwave Theory and Techniques, 2016, 64, 4274-4286.	2.9	67
43	Digitally Modulated CMOS Polar Transmitters for Highly-Efficient mm-Wave Wireless Communication. IEEE Journal of Solid-State Circuits, 2016, 51, 1579-1592.	3.5	49
44	A DTC-Based Subsampling PLL Capable of Self-Calibrated Fractional Synthesis and Two-Point Modulation. IEEE Journal of Solid-State Circuits, 2016, 51, 3078-3092.	3.5	50
45	A 150 kHzâ€“80 MHz BW Discrete-Time Analog Baseband for Software-Defined-Radio Receivers using a 5th-Order IIR LPF, Active FIR and a 10 bit 300 MS/s ADC in 28 nm CMOS. IEEE Journal of Solid-State Circuits, 2016, 51, 1593-1606.	3.5	14
46	An 80 GHz Low-Noise Amplifier Resilient to the TX Spillover in Phase-Modulated Continuous-Wave Radars. IEEE Journal of Solid-State Circuits, 2016, 51, 1141-1153.	3.5	38
47	A Comprehensive Benchmark and Optimization of 5-nm Lateral and Vertical GAA 6T-SRAMs. IEEE Transactions on Electron Devices, 2016, 63, 643-651.	1.6	26
48	A 6x-oversampling 10GS/s 60GHz polar transmitter with 15.3% average PA efficiency in 40nm CMOS. , 2015, , .		4
49	An electrical-balance duplexer for in-band full-duplex with <-85dBm in-band distortion at +10dBm TX-power. , 2015, , .		11
50	A Wideband Beamforming Lowpass Filter for 60 GHz Phased-Array Receivers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2324-2333.	3.5	7
51	An 80-GHz low noise amplifier resilient to the TX-spillover in phase-modulated continuous-wave radars. , 2015, , .		3
52	Flicker noise upconversion mechanisms in K-band CMOS VCOs. , 2015, , .		14
53	A 150 kHz-80 MHz BW DT analog baseband for SDR RX using a 5th-order IIR LPF, active FIR and 10b 300 MS/s ADC in 28nm CMOS. , 2015, , .		2
54	A 42 mW 200 fs-Jitter 60 GHz Sub-Sampling PLL in 40 nm CMOS. IEEE Journal of Solid-State Circuits, 2015, 50, 2025-2036.	3.5	47

#	Article	IF	Citations
55	An Incremental-Charge-Based Digital Transmitter With Built-in Filtering. IEEE Journal of Solid-State Circuits, 2015, 50, 3065-3076.	3.5	24
56	Design and Tuning of Coupled-LC mm-Wave Subharmonically Injection-Locked Oscillators. IEEE Transactions on Microwave Theory and Techniques, 2015, 63, 2301-2312.	2.9	26
57	A 10-bit, 550-fs step Digital-to-Time Converter in 28nm CMOS. , 2014, , .		51
58	A Low-Power Analog Baseband Section for 60-GHz Receivers in 90-nm CMOS. IEEE Transactions on Microwave Theory and Techniques, 2014, 62, 1724-1735.	2.9	15
59	A 4.1-mW 3.5-GS/s 6-Bit Time-Interleaved ADC in 40-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 466-470.	2.2	2
60	A 70 dB DR 10 b 0-to-80 MS/s Current-Integrating SAR ADC With Adaptive Dynamic Range. IEEE Journal of Solid-State Circuits, 2014, 49, 1173-1183.	3.5	35
61	A 79 GHz Phase-Modulated 4 GHz-BW CW Radar Transmitter in 28 nm CMOS. IEEE Journal of Solid-State Circuits, 2014, 49, 2925-2937.	3.5	82
62	A mm-wave 40 nm CMOS subharmonically injection-locked QVCO with lock detection. , 2013, , .		3
63	Analog baseband beamformer for use in a phased-array 60 GHz transmitter. , 2012, , .		1
64	A CMOS IQ Digital Doherty Transmitter using modulated tuning capacitors. , 2012, , .		26
65	A 42mW wideband baseband receiver section with beamforming functionality for 60GHz applications in 40nm low-power CMOS. , 2012, , .		10
66	A 2.6 mW 6 bit 2.2 GS/s Fully Dynamic Pipeline ADC in 40 nm Digital CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 2080-2090.	3.5	99
67	A Fully Integrated 7.3 kV HBM ESD-Protected Transformer-Based 4.5â€“6 GHz CMOS LNA. IEEE Journal of Solid-State Circuits, 2009, 44, 344-353.	3.5	27
68	A 2.2 mW 1.75 GS/s 5 Bit Folding Flash ADC in 90 nm Digital CMOS. IEEE Journal of Solid-State Circuits, 2009, 44, 874-882.	3.5	64
69	A Low-Complexity, Low-Phase-Noise, Low-Voltage Phase-Aligned Ring Oscillator in 90 nm Digital CMOS. IEEE Journal of Solid-State Circuits, 2009, 44, 1942-1949.	3.5	28
70	A 52 GHz Phased-Array Receiver Front-End in 90 nm Digital CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 2651-2659.	3.5	89
71	A Compact Wideband Front-End Using a Single-Inductor Dual-Band VCO in 90 nm Digital CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 2693-2705.	3.5	45
72	Low-Area Active-Feedback Low-Noise Amplifier Design in Scaled Digital CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 2422-2433.	3.5	155

#	Article	IF	Citations
73	A 100-kHz to 20-MHz Reconfigurable Power-Linearity Optimized G_mâ€“C Biquad in 0.13-mum CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 224-228.	2.2	20
74	A CMOS Ultra-Wideband Receiver for Low Data-Rate Communication. IEEE Journal of Solid-State Circuits, 2007, 42, 2515-2527.	3.5	63
75	Indoor body-area channel model for narrowband communications. IET Microwaves, Antennas and Propagation, 2007, 1, 1197.	0.7	69
76	The Potential of FinFETs for Analog and RF Circuit Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2007, 54, 2541-2551.	3.5	40
77	Modeling of Substrate Noise Generation, Isolation, and Impact for an LC-VCO and a Digital Modem on a Lightly-Doped Substrate. IEEE Journal of Solid-State Circuits, 2006, 41, 2040-2051.	3.5	19
78	Ultra-wideband channel model for communication around the human body. IEEE Journal on Selected Areas in Communications, 2006, 24, 927-933.	9.7	249
79	An ultra-wideband body area propagation channel Model-from statistics to implementation. IEEE Transactions on Microwave Theory and Techniques, 2006, 54, 1820-1826.	2.9	227
80	Planar Bulk MOSFETs Versus FinFETs: An Analog/RF Perspective. IEEE Transactions on Electron Devices, 2006, 53, 3071-3079.	1.6	128
81	SWAN: high-level simulation methodology for digital substrate noise generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 23-33.	2.1	23
82	ESDâ€“RF co-design methodology for the state of the art RF-CMOS blocks. Microelectronics Reliability, 2005, 45, 255-268.	0.9	11
83	Low-power voltage-controlled oscillators in 90-nm CMOS using high-quality thin-film postprocessed inductors. IEEE Journal of Solid-State Circuits, 2005, 40, 1922-1931.	3.5	24
84	Performance degradation of LC-tank VCOs by impact of digital switching noise in lightly doped substrates. IEEE Journal of Solid-State Circuits, 2005, 40, 1472-1481.	3.5	38
85	A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS. IEEE Journal of Solid-State Circuits, 2005, 40, 1434-1442.	3.5	124
86	Digital circuit capacitance and switching analysis for ground bounce in ICs with a high-ohmic substrate. IEEE Journal of Solid-State Circuits, 2004, 39, 1119-1130.	3.5	25
87	Gate-source-drain architecture impact on DC and RF performance of sub-100-nm elevated source/drain NMOS transistors. IEEE Transactions on Electron Devices, 2003, 50, 610-617.	1.6	9
88	Analysis and experimental verification of digital substrate noise generation for epi-type substrates. IEEE Journal of Solid-State Circuits, 2000, 35, 1002-1008.	3.5	125
89	Efficient symbolic computation of approximated small-signal characteristics of analog integrated circuits. IEEE Journal of Solid-State Circuits, 1995, 30, 327-330.	3.5	71
90	On the relationship between the CMRR or PSRR and the second harmonic distortion of differential input amplifiers. IEEE Journal of Solid-State Circuits, 1989, 24, 1740-1744.	3.5	23