

Jinwoo Kim

List of Publications by Year in descending order

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11
papers

117
citations

1684188

5
h-index

2053705

5
g-index

11
all docs

11
docs citations

11
times ranked

90
citing authors

#	ARTICLE	IF	CITATIONS
1	Worst-Case Eye Analysis of High-Speed Channels Based on Bayesian Optimization. IEEE Transactions on Electromagnetic Compatibility, 2021, 63, 246-258.	2.2	7
2	Chiplet/Interposer Co-Design for Power Delivery Network Optimization in Heterogeneous 2.5-D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 2148-2157.	2.5	5
3	An Effective Block Pin Assignment Approach for Block-Level Monolithic 3-D ICs. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 26-34.	1.5	0
4	An SRAM Compiler for Monolithic-3D Integrated Circuit with Carbon Nanotube Transistors. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, , 1-1.	1.5	1
5	ParaMitE: Mitigating Parasitic CNFETs in the Presence of Unetched CNTs. , 2021, , .		0
6	Advances in Design and Test of Monolithic 3-D ICs. IEEE Design and Test, 2020, 37, 92-100.	1.2	6
7	Architecture, Chip, and Package Codesign Flow for Interposer-Based 2.5-D Chiplet Integration Enabling Heterogeneous IP Reuse. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2424-2437.	3.1	32
8	Design Flow for Active Interposer-Based 2.5-D ICs and Study of RISC-V Architecture With Secure NoC. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 2047-2060.	2.5	7
9	Architecture, Chip, and Package Co-design Flow for 2.5D IC Design Enabling Heterogeneous IP Reuse. , 2019, , .		33
10	RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs. , 2019, , .		8
11	A Spectral Convolutional Net for Co-Optimization of Integrated Voltage Regulators and Embedded Inductors. , 2019, , .		18