Chulwoo Kim

List of Publications by Year
in descending order

62	742	623734	552781
papers	citations	14 h-index	26 g-index

62	62	62	742
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A DCâ€“DC Boost Converter With Variation-Tolerant MPPT Technique and Efficient ZCS Circuit for Thermoelectric Energy Harvesting Applications. IEEE Transactions on Power Electronics, 2013, 28, 3827-3833.	7.9	134
2	Self-Powered 30 ÂµW to 10 mW Piezoelectric Energy Harvesting System With 9.09 ms/V Maximum Power Point Tracking Time. IEEE Journal of Solid-State Circuits, 2015, 50, 2367-2379.	5.4	92
3	Edge-Pursuit Comparator: An Energy-Scalable Oscillator Collapse-Based Comparator With Application in a 74.1 dB SNDR and 20 kS/s 15 b SAR ADC. IEEE Journal of Solid-State Circuits, 2017, 52, 1077-1090.	5.4	58
4	3-Gb/s High-Speed True Random Number Generator Using Common-Mode Operating Comparator and Sampling Uncertainty of D Flip-Flop. IEEE Journal of Solid-State Circuits, 2017, 52, 605-610.	5.4	36
5	A High-Voltage Dual-Input Buck Converter Achieving 52.9% Maximum End-to-End Efficiency for Triboelectric Energy-Harvesting Applications. IEEE Journal of Solid-State Circuits, 2020, 55, 1324-1336.	5.4	26
6	A 1.0-ns/1.0-V Delay-Locked Loop With Racing Mode and Countered CAS Latency Controller for DRAM Interfaces. IEEE Journal of Solid-State Circuits, 2012, 47, 1436-1447.	5.4	25
7	A High-Efficiency Charger With Adaptive Input Ripple MPPT for Low-Power Thermoelectric Energy Harvesting Achieving 21% Efficiency Improvement. IEEE Transactions on Power Electronics, 2020, 35, 347-358.	7.9	22
8	A 90.2% Peak Efficiency Multi-Input Single-Inductor Multi-Output Energy Harvesting Interface With Double-Conversion Rejection Technique and Buck-Based Dual-Conversion Mode. IEEE Journal of Solid-State Circuits, 2021, 56, 961-971.	5.4	22
9	An Antiharmonic, Programmable, DLL-Based Frequency Multiplier for Dynamic Frequency Scaling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1130-1134.	3.1	21
10	A 3.5 GHz Spread-Spectrum Clock Generator With a Memoryless Newton-Raphson Modulation Profile. IEEE Journal of Solid-State Circuits, 2012, 47, 1199-1208.	5.4	18
11	30-Gb/s 1.11-pJ/bit Single-Ended PAM-3 Transceiver for High-Speed Memory Links. IEEE Journal of Solid-State Circuits, 2021, 56, 581-590.	5.4	17
12	A High-Voltage Dual-Input Buck Converter With Bidirectional Inductor Current for Triboelectric Energy-Harvesting Applications. IEEE Journal of Solid-State Circuits, 2021, 56, 541-553.	5.4	17
13	A 1-V 10-Gb/s/pin Single-Ended Transceiver With Controllable Active-Inductor-Based Driver and Adaptively Calibrated Cascaded-Equalizer for Post-LPDDR4 Interfaces. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 331-342.	5.4	15
14	A Near-Threshold Voltage Oriented Digital Cell Library for High-Energy Efficiency and Optimized Performance in 65nm CMOS Process. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1567-1580.	5.4	14
15	A 0.5 V 10-bit 3 MS/s SAR ADC With Adaptive-Reset Switching Scheme and Near-Threshold Voltage-Optimized Design Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1184-1188.	3.0	14
16	A 247 ÂµW 800 Mb/s/pin DLL-Based Data Self-Aligner for Through Silicon via (TSV) Interface. IEEE Journal of Solid-State Circuits, 2013, 48, 711-723.	5.4	13
17	A Dual-Mode Continuously Scalable-Conversion-Ratio SC Energy Harvesting Interface With SC-Based PFM MPPT and Flying Capacitor Sharing Scheme. IEEE Journal of Solid-State Circuits, 2021, 56, 2724-2735.	5.4	13
18	Survey and Analysis of Delay-Locked Loops Used in DRAM Interfaces. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 701-711.	3.1	12

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19	A 1.62â€“5.4-Gb/s Receiver for DisplayPort Version 1.2a With Adaptive Equalization and Referenceless Frequency Acquisition Techniques. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2691-2702.	5.4	12
20	Fully Integrated Low-Power Energy Harvesting System With Simplified Ripple Correlation Control for System-on-a-Chip Applications. IEEE Transactions on Power Electronics, 2019, 34, 4353-4361.	7.9	12
21	Piecewise Linear Modulation Technique for Spread Spectrum Clock Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1234-1245.	3.1	11
22	An 11-b 100-MS/s Fully Dynamic Pipelined ADC Using a High-Linearity Dynamic Amplifier. IEEE Journal of Solid-State Circuits, 2020, 55, 2468-2477.	5.4	10
23	A 1.3â€“4-GHz Quadrature-Phase Digital DLL Using Sequential Delay Control and Reconfigurable Delay Line. IEEE Journal of Solid-State Circuits, 2021, 56, 1886-1896.	5.4	10
24	An oscillator collapse-based comparator with application in a 74.1dB SNDR, 20KS/s 15b SAR ADC. , 2016, , .		9
25	An Efficiency-Aware Cooperative Multicharger System for Photovoltaic Energy Harvesting Achieving 14% Efficiency Improvement. IEEE Transactions on Power Electronics, 2020, 35, 2253-2256.	7.9	8
26	A Periodically Refreshed Capacitive Floating Level Shifter for Conditional Switching Applications. IEEE Transactions on Power Electronics, 2021, 36, 1264-1268.	7.9	8
27	A 5-GHz Subsampling PLL-Based Spread-Spectrum Clock Generator by Calibrating the Frequency Deviation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1132-1136.	3.0	7
28	A Bidirectional High-Voltage Dual-Input Buck Converter for Triboelectric Energy-Harvesting Interface Achieving 70.72% End-to-End Efficiency. , 2019, , .		7
29	A Four-Phase Hybrid Step-Up/Down Converter With RMS Inductor Current Reduction and Delay-Based Zero-Current Detection. IEEE Transactions on Power Electronics, 2022, 37, 3708-3712.	7.9	7
30	A 0.0018Âmm2 frequency-to-digital-converter-based CMOS smart temperature sensor. Analog Integrated Circuits and Signal Processing, 2010, 64, 153-157.	1.4	6
31	A DLL-Based Quadrature Clock Generator With a 3-Stage Quad Delay Unit Using the Sub-Range Phase Interpolator for Low-Jitter and High-Phase Accuracy DRAM Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2342-2346.	3.0	6
32	A 56-Gb/s PAM-4 Receiver Using Time-Based LSB Decoder and S/H Technique for Robustness to Comparator Voltage Variations. IEEE Journal of Solid-State Circuits, 2022, 57, 562-572.	5.4	6
33	A 0.99-pJ/b 15-Gb/s Counter-Based Adaptive Equalizer Using Single Comparator in 28-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3189-3193.	3.0	6
34	12-Gb/s Over Four Balanced Lines Utilizing NRZ Braid Clock Signaling With No Data Overhead and Spread Transition Scheme for 8K UHD Intra-Panel Interfaces. IEEE Journal of Solid-State Circuits, 2019, 54, 463-475.	5.4	5
35	A Low-Power Post-LPDDR4 Interface Using AC Termination at RX and an Active Inductor at TX. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 789-793.	3.0	4
36	A 9-bit 500-MS/s 2-bit/cycle SAR ADC With Error-Tolerant Interpolation Technique. IEEE Journal of Solid-State Circuits, 2022, 57, 1492-1503.	5.4	4

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37	A Hybrid DC-DC Converter Capable of Supplying Heavy Load in Step-Up and Step-Down Mode. , 2021, , .		4
38	A Capacitively Coupled CT Î” Î£M With Chopping Artifacts Rejection for Sensor Readout ICs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3242-3253.	5.4	4
39	A 15 Gb/s Non-Return-to-Zero Transmitter With 1-Tap Pre-Emphasis Feed-Forward Equalizer for Low-Power Ground Terminated Memory Interfaces. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2737-2741.	3.0	4
40	A Sub-fs-FoM Digital LDO Using PMOS and NMOS Arrays With Fully Integrated 7.2-pF Total Capacitance. IEEE Journal of Solid-State Circuits, 2019, , 1-13.	5.4	3
41	A 25 Gb/s Wireline Receiver With Feedforward and Feedback Equalizers at Analog Front-End. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 404-408.	3.0	3
42	An 88.9-dB SNR Fully-Dynamic Noise-Shaping SAR Capacitance-to-Digital Converter. IEEE Journal of Solid-State Circuits, 2022, 57, 2778-2790.	5.4	3
43	Differential pass transistor pulsed latch. Electrical Engineering, 2007, 89, 371-375.	2.0	2
44	A 3ÂGb/s transmitter with a tapless pre-emphasis CML output driver. Analog Integrated Circuits and Signal Processing, 2014, 81, 461-469.	1.4	2
45	A $DeltaSigma$ Modulator-Based Spread-Spectrum Clock Generator with Digital Compensation and Calibration for Phase-Locked Loop Bandwidth. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 192-196.	3.0	2
46	Analysis of a Multiwire, Multilevel, and Symbol Correlation Combination Scheme. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 3416-3427.	5.4	2
47	Railâ€toâ€rail regulating voltageâ€controlled oscillator with low supply and ground noise sensitivity. Electronics Letters, 2015, 51, 1980-1982.	1.0	1
48	A Spread Spectrum Clock Generator With Nested Modulation Profile for a High-Resolution Display System. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1509-1513.	3.0	1
49	Near threshold voltage digital PLL using low voltage optimised blocks for AR display system. IET Circuits, Devices and Systems, 2020, 14, 155-158.	1.4	1
50	A 1.69-pJ/b 14-Gb/s Digital Sub-Sampling CDR With Combined Adaptive Equalizer and Self-Error Corrector. IEEE Access, 2021, 9, 118907-118918.	4.2	1
51	A 2.4â€“8 GHz Phase Rotator Delay-Locked Loop Using Cascading Structure for Direct Inputâ€“Output Phase Detection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 794-798.	3.0	1
52	A 1 MS/s 9.15 ENOB Low-Power SAR ADC with Triple-Charge-Sharing Technique. , 2020, , .		1
53	A CMOS optical receiver with subtraction-based level shifter for high-definition digital audio interfaces. Analog Integrated Circuits and Signal Processing, 2007, 51, 169-173.	1.4	0
54	Highâ€performance wideâ€V DDH â€range level converter for mixedâ€signal systems. Electronics Letters, 2013, 49, 1125-1126.	1.0	0

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55	A 6ÂGb/s transmitter with data-dependent jitter reduction technique for displayport physical layer. Analog Integrated Circuits and Signal Processing, 2014, 81, 529-536.	1.4	0
56	2.56ÂGHz subâ€harmonically injectionâ€locked PLL with cascaded DLL for multiâ€phase injection. Electronics Letters, 2014, 50, 1803-1804.	1.0	0
57	A 400ÂMHzâ€“1.5ÂGHz all digital integer-N PLL with a reference spur reduction technique. Analog Integrated Circuits and Signal Processing, 2014, 79, 183-189.	1.4	0
58	A 10 Gbits/s/pin DFE-Less Graphics DRAM Interface With Adaptive-Bandwidth PLL for Avoiding Noise Interference and CIJ Reduction Technique. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 344-353.	3.1	0
59	An Area-Efficient and Wide-Range Inter-Signal Skew Compensation Scheme With the Embedded Bypass Control Register Operating as a Binary Search Algorithm for DRAM Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1775-1779.	3.0	0
60	A Power Management System Based on Adaptive Low-Dropout Voltage Regulator with Optimal Reference Pre-Compensation Technique. , 2021, , .		0
61	A 0.37â€in. 5900PPI liquid crystal on silicon CMOS SoC using low voltage high dynamic voltage range novel pixel circuit for augmented reality microâ€displays. Journal of the Society for Information Display, 2021, 29, 785.	2.1	0
62	A 32-Gb/s Dual-Mode Transceiver With One-Tap FIR and Two-Tap IIR RX Only Equalization in 65-nm CMOS Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1567-1574.	3.1	0