Yu Lei

List of Publications by Year
in descending order

24	83	1937685 4	1474206 9
papers	citations	h-index	g-index

24	24	24	64
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Enhancing the Performance of Phase Change Memory for Embedded Applications. Physica Status Solidi - Rapid Research Letters, 2019, 13, 1800558.	2.4	30
2	An emission stable vertical air channel diode by a low-cost and IC compatible BOE etching process. Nanoscale, 2021, 13, 5693-5699.	5.6	12
3	BIST-Based Fault Diagnosis for PCM With Enhanced Test Scheme and Fault-Free Region Finding Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1652-1664.	3.1	6
4	An Ultra-Low Quiescent Current Resistor-Less Power on Reset Circuit. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 146-150.	3.0	5
5	A Single-Reference Parasitic-Matching Sensing Circuit for 3-D Cross Point PCM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 486-490.	3.0	4
6	A smart primary side current sensing strategy for single stage isolated PFC controller. IEICE Electronics Express, 2015, 12, 20150901-20150901.	0.8	3
7	Enhanced 3 Ã— VDD-tolerant ESD clamp circuit with stacked configuration. IEICE Electronics Express, 2017, 14, 20160901-20160901.	0.8	3
8	A novel high performance 3Ã—VDD-tolerant ESD detection circuit in advanced CMOS process. IEICE Electronics Express, 2017, 14, 20170899-20170899.	0.8	3
9	2V/3 Bias Scheme with Enhanced Dynamic Read Performances for 3-D Cross Point PCM. , 2020, , .		3
10	MPPT Circuit Using Time Exponential Rate Perturbation and Observation for Enhanced Tracking Efficiency for a Wide Resistance Range of Thermoelectric Generator. Applied Sciences (Switzerland), 2021, 11, 4650.	2.5	3
11	Enhanced read performance for phase change memory using a reference column. IEICE Electronics Express, 2017, 14, 20170032-20170032.	0.8	2
12	A Changing-Reference Parasitic-Matching Sensing Circuit for 3-D Vertical RRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1268-1276.	3.1	2
13	Silicon Modeling of Spiking Neurons With Diverse Dynamic Behaviors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2199-2212.	2.7	2
14	Set/reset reference and parasitic matching scheme to speed up PCM read operation. Electronics Letters, 2017, 53, 144-146.	1.0	1
15	Capacitor-less LDR based on flipped voltage follower with dual-feedback loops. IEICE Electronics Express, 2017, 14, 20170496-20170496.	0.8	1
16	The Influence of the Bitline Length on the Resistance Consistency in Phase Change Memory Array. ECS Journal of Solid State Science and Technology, 2018, 7, Q33-Q37.	1.8	1
17	Nanoscale Sensors Based on Field Emission Mechanism in Air. , 2019, , .		1
18	Near-threshold SIDO DC-DC converter with a high-precision ZCD for phase change memory chip. IEICE Electronics Express, 2019, 16, 20190250-20190250.	0.8	1

#	Article	IF	Citations
19	High speed sense amplifier with efficient pre-charge scheme for PCM in the 28nm process. , 2016, , .		0
20	Optimization of a PCRAM Chip for high-speed read and highly reliable reset operations. , 2016, , .		0
21	An efficiency-enhanced 2X/1.5X SC charge pump with auto-adjustable output regulation for PCM. Proceedings of SPIE, 2016, , .	0.8	0
22	Nanoscale Manipulation for The Fabrication of Field-emission Air-channel Transistors. , 2019, , .		0
23	A Near-Accurate-Parasitic-Balancing Sensing Scheme for PCM With 8.9-ns Read Access Time and 16.2-nsÂ·pJ/Kb FoM. IEEE Solid-State Circuits Letters, 2020, 3, 510-513.	2.0	0
24	A self-start circuit with asymmetric inductors reconfigurable technology for dual-output boost converter for energy harvesting. IEICE Electronics Express, 2020, 17, 20200284-20200284.	0.8	0