## Kuan-Neng Chen

List of Publications by Year in descending order

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#	Article	IF	CITATIONS
1	Wafer-level bonding/stacking technology for 3D integration. Microelectronics Reliability, 2010, 50, 481-488.	1.7	163
2	Low temperature bonding technology for 3D integration. Microelectronics Reliability, 2012, 52, 302-311.	1.7	132
3	Low-temperature direct copper-to-copper bonding enabled by creep on (111) surfaces of nanotwinned Cu. Scientific Reports, 2015, 5, 9734.	3.3	120
4	Three-Dimensional Integrated Circuit (3D IC) Key Technology: Through-Silicon Via (TSV). Nanoscale Research Letters, 2017, 12, 56.	5.7	112
5	Wafer-level Cu–Cu bonding technology. Microelectronics Reliability, 2012, 52, 312-320.	1.7	100
6	Microstructure evolution and abnormal grain growth during copper wafer bonding. Applied Physics Letters, 2002, 81, 3774-3776.	3.3	96
7	Low-temperature direct copper-to-copper bonding enabled by creep on highly (111)-oriented Cu surfaces. Scripta Materialia, 2014, 78-79, 65-68.	5.2	89
8	Fabrication technologies for three-dimensional integrated circuits. , 0, , .		83
9	Novel Cu-to-Cu Bonding With Ti Passivation at 180\$^{circ}{m C}\$ in 3-D Integration. IEEE Electron Device Letters, 2013, 34, 1551-1553.	3.9	82
10	Materials challenges in three-dimensional integrated circuits. MRS Bulletin, 2015, 40, 219-222.	3.5	69
11	Comparisons of Conventional, 3-D, Optical, and RF Interconnects for On-Chip Clock Distribution. IEEE Transactions on Electron Devices, 2004, 51, 233-239.	3.0	68
12	Demonstration and Electrical Performance of Cu–Cu Bonding at 150 °C With Pd Passivation. IEEE Transactions on Electron Devices, 2015, 62, 2587-2592.	3.0	65
13	Microstructure examination of copper wafer bonding. Journal of Electronic Materials, 2001, 30, 331-335.	2.2	63
14	Contact Resistance Measurement of Bonded Copper Interconnects for Three-Dimensional Integration Technology. IEEE Electron Device Letters, 2004, 25, 10-12.	3.9	62
15	Bonding parameters of blanket copper wafer bonding. Journal of Electronic Materials, 2006, 35, 230-234.	2.2	61
16	Vertical interconnects of microbumps in 3D integration. MRS Bulletin, 2015, 40, 257-263.	3.5	59
17	Low Temperature Cu–Cu Bonding Technology in Three-Dimensional Integration: An Extensive Review. Journal of Electronic Packaging, Transactions of the ASME, 2018, 140, .	1.8	59
18	Structure, Design and Process Control for Cu Bonded Interconnects in 3D Integrated Circuits. , 2006,		56

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19	Wafer-to-Wafer Alignment for Three-Dimensional Integration: A Review. Journal of Microelectromechanical Systems, 2011, 20, 885-898.	2.5	56
20	Reliability of key technologies in 3D integration. Microelectronics Reliability, 2013, 53, 7-16.	1.7	46
21	Wafer-level three-dimensional integrated circuits (3D IC): Schemes and key technologies. Microelectronic Engineering, 2011, 88, 3282-3286.	2.4	36
22	Integration schemes and enabling technologies for three-dimensional integrated circuits. IET Computers and Digital Techniques, 2011, 5, 160.	1.2	31
23	Development of low temperature Cu Cu bonding and hybrid bonding for three-dimensional integrated circuits (3D IC). Microelectronics Reliability, 2021, 127, 114412.	1.7	30
24	Crosstalk evaluation, suppression and modeling in 3D through-strata-via (TSV) network. , 2010, , .		29
25	Demonstration and Electrical Performance Investigation of Wafer-Level Cu Oxide Hybrid Bonding Schemes. IEEE Electron Device Letters, 2011, 32, 1119-1121.	3.9	29
26	Electrical and Reliability Investigation of Cu-to-Cu Bonding With Silver Passivation Layer in 3-D Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 36-42.	2.5	28
27	A precise pH microsensor using RF-sputtering IrO2 and Ta2O5 films on Pt-electrode. Sensors and Actuators B: Chemical, 2014, 193, 687-691.	7.8	27
28	Demonstration of Low-Temperature Fine-Pitch Cu/SiOâ,, Hybrid Bonding by Au Passivation. IEEE Journal of the Electron Devices Society, 2021, 9, 868-875.	2.1	26
29	Thermal stress effects of Ge2Sb2Te5 phase change material: Irreversible modification with Ti adhesion layers and segregation of Te. Microelectronic Engineering, 2008, 85, 2346-2349.	2.4	24
30	Electrical and Reliability Investigation of Cu TSVs With Low-Temperature Cu/Sn and BCB Hybrid Bond Scheme. IEEE Electron Device Letters, 2013, 34, 102-104.	3.9	23
31	Low-Temperature Direct CVD Oxides to Thermal Oxide Wafer Bonding in Silicon Layer Transfer. Electrochemical and Solid-State Letters, 2005, 8, G1.	2.2	22
32	Investigation of bonding mechanism for low-temperature Cu Cu bonding with passivation layer. Applied Surface Science, 2022, 592, 153243.	6.1	22
33	Submicron Cu/Sn Bonding Technology With Transient Ni Diffusion Buffer Layer for 3DIC Application. IEEE Electron Device Letters, 2014, 35, 1118-1120.	3.9	20
34	A Wafer-Level Three-Dimensional Integration Scheme With Cu TSVs Based on Microbump/Adhesive Hybrid Bonding for Three-Dimensional Memory Application. IEEE Transactions on Device and Materials Reliability, 2012, 12, 209-216.	2.0	19
35	Cosputtered Cu/Ti Bonded Interconnects With a Self-Formed Adhesion Layer for Three-Dimensional Integration Applications. IEEE Electron Device Letters, 2012, 33, 1048-1050.	3.9	19
36	Controlled large strain of Ni silicide/Si/Ni silicide nanowire heterostructures and their electron transport properties. Applied Physics Letters, 2010, 97, 203110.	3.3	17

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37	Asymmetric Wafer-Level Polyimide and Cu/Sn Hybrid Bonding for 3-D Heterogeneous Integration. IEEE Transactions on Electron Devices, 2019, 66, 3073-3079.	3.0	17
38	Low Temperature Copper-Copper Bonding of Non-Planarized Copper Pillar With Passivation. IEEE Electron Device Letters, 2020, 41, 1229-1232.	3.9	17
39	Wafer-level 3D integration using hybrid bonding. , 2010, , .		16
40	Location-controlled-grain Technique for Monolithic 3D BEOL FinFET Circuits. , 2018, , .		16
41	Monolithic 3D BEOL FinFET switch arrays using location-controlled-grain technique in voltage regulator with better FOM than 2D regulators. , 2019, , .		16
42	Investigation of Low-Temperature Cu–Cu Direct Bonding With Pt Passivation Layer in 3-D Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 573-578.	2.5	16
43	Sealing Bump With Bottom-Up Cu TSV Plating Fabrication in 3-D Integration Scheme. IEEE Electron Device Letters, 2013, 34, 671-673.	3.9	15
44	Modeling and Characterization of TSV Capacitor and Stable Low-Capacitance Implementation for Wide-I/O Application. IEEE Transactions on Device and Materials Reliability, 2015, 15, 129-135.	2.0	15
45	An RDL-First Fan-out Wafer Level Package for Heterogeneous Integration Applications. , 2018, , .		15
46	An Advanced 2.5-D Heterogeneous Integration Packaging for High-Density Neural Sensing Microsystem. IEEE Transactions on Electron Devices, 2017, 64, 1666-1673.	3.0	14
47	Low-Temperature (70°C) Cu-to-Cu Direct Bonding by Capping Metal Layers. IEEE Electron Device Letters, 2021, 42, 1524-1527.	3.9	14
48	Direct metal bonding using nanotwinned Ag films with (1 1 1) surface orientation under air atmosphere for heterogeneous integration. Applied Surface Science, 2022, 576, 151845.	6.1	14
49	A Flexible pH-Sensing Structure Using WO3/IrO2 Junction with Al2O3 Encapsulation Layer. ECS Solid State Letters, 2012, 2, P28-P30.	1.4	13
50	Low-Temperature Cu–Cu Direct Bonding Using Pillar–Concave Structure in Advanced 3-D Heterogeneous Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 7, 1560-1566.	2.5	13
51	Optimization of Laser Release Process for Throughput Enhancement of Fan-Out Wafer-Level Packaging. , 2018, , .		13
52	Atomic Layer Deposition Plasma-Based Undoped-HfO <sub>2</sub> Ferroelectric FETs for Non-Volatile Memory. IEEE Electron Device Letters, 2021, 42, 1152-1155.	3.9	13
53	A double-sided, single-chip integration scheme using through-silicon-via for neural sensing applications. Biomedical Microdevices, 2015, 17, 11.	2.8	12
54	3-D Stacked Technology of DRAM-Logic Controller Using Through-Silicon Via (TSV). IEEE Journal of the Electron Devices Society, 2018, 6, 396-402.	2.1	12

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55	Low-Temperature Bonded Cu/In Interconnect With High Thermal Stability for 3-D Integration. IEEE Transactions on Electron Devices, 2014, 61, 1131-1136.	3.0	11
56	Backside-Process-Induced Junction Leakage and Process Improvement of Cu TSV Based on Cu/Sn and BCB Hybrid Bonding. IEEE Electron Device Letters, 2013, 34, 435-437.	3.9	10
57	A Novel 3D Integration Scheme for Backside Illuminated CMOS Image Sensor Devices. IEEE Transactions on Device and Materials Reliability, 2014, 14, 715-720.	2.0	10
58	Motional Resistance Issue of TSV-Based Resonator Device and Its Improvement With a Concave Cu TSV Structural Design. IEEE Electron Device Letters, 2014, 35, 865-867.	3.9	10
59	Ultrahigh-Density 256-Channel Neural Sensing Microsystem Using TSV-Embedded Neural Probes. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 1013-1025.	4.0	10
60	Electrical Performance and Reliability Investigation of Cosputtered Cu/Ti Bonded Interconnects. IEEE Transactions on Electron Devices, 2013, 60, 3521-3526.	3.0	9
61	Advanced TSV-Based Crystal Resonator Devices Using 3-D Integration Scheme With Hermetic Sealing. IEEE Electron Device Letters, 2013, 34, 1041-1043.	3.9	9
62	<pre>\$hbox{Al}_{2}hbox{O}_{3}\$ Interface Engineering of Germanium Epitaxial Layer Grown Directly on Silicon. IEEE Transactions on Electron Devices, 2013, 60, 56-62.</pre>	3.0	9
63	Low-temperature and low-pressure direct copper-to-copper bonding by highly (111)-oriented nanotwinned Cu. , 2016, , .		9
64	Process Development and Material Characteristics of TSV-Less Interconnection Technology for FOWLP. , 2017, , .		9
65	Robust terahertz polarizers with high transmittance at selected frequencies through Si wafer bonding technologies. Optics Letters, 2017, 42, 4917.	3.3	9
66	A Novel Low-Temperature Cu-Cu Direct Bonding with Cr Wetting Layer and Au Passivation Layer. , 2020, , .		9
67	Electrical Characteristics and Reliability of Wafer-on-Wafer (WOW) Bumpless Through-Silicon Via. IEEE Transactions on Electron Devices, 2021, 68, 3520-3525.	3.0	9
68	BCB-to-oxide bonding technology for 3D integration. Microelectronics Reliability, 2012, 52, 352-355.	1.7	8
69	2.5D Heterogeneously Integrated Microsystem for High-Density Neural Sensing Applications. IEEE Transactions on Biomedical Circuits and Systems, 2014, 8, 810-823.	4.0	8
70	Investigation and Optimization of Ultrathin Buffer Layers Used in Cu/Sn Eutectic Bonding. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 1225-1230.	2.5	8
71	Adhesion Investigation Between Metal and Benzocyclobutene (BCB) Polymer Dielectric Materials in 3-D Integration Applications. IEEE Transactions on Device and Materials Reliability, 2014, 14, 914-920.	2.0	7
72	Development and electrical investigation of novel fine-pitch Cu/Sn pad bumping using ultra- thin buffer layer technique in 3D integration. , 2015, , .		7

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73	Development of Bumpless Stacking With Bottom–Up TSV Fabrication. IEEE Transactions on Electron Devices, 2017, 64, 1660-1665.	3.0	7
74	Low Temperature Cu to Cu Direct Bonding below 150 $\hat{A}^oC$ with Au Passivation Layer. , 2019, , .		7
75	Ferroelectric Undoped HfO <sub> <i>x</i> </sub> Capacitor With Symmetric Synaptic for Neural Network Accelerator. IEEE Transactions on Electron Devices, 2021, 68, 1374-1377.	3.0	7
76	Wafer-to-wafer hybrid bonding technology for 3D IC. , 2010, , .		6
77	Low temperature (<180°C) wafer-level and chip-level In-to-Cu and Cu-to-Cu bonding for 3D integration. , 2013, , .		6
78	Through-silicon-via-based double-side integrated microsystem for neural sensing applications. , 2013, , .		6
79	Energy-efficient low-noise 16-channel analog-front-end circuit for bio-potential acquisition. , 2014, , .		6
80	Conductivity enhancement of multiwalled carbon nanotube thin film via thermal compression method. Nanoscale Research Letters, 2014, 9, 451.	5.7	6
81	A Novel Bonding Approach and Its Electrical Performance for Flexible Substrate Integration. IEEE Journal of the Electron Devices Society, 2016, 4, 185-188.	2.1	6
82	Characterization of Temporary Bonding and Laser Release Using Polyimide and a 300-nm Photolysis Polymer System for High-Throughput 3-D IC Applications. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 7, 456-462.	2.5	6
83	A Novel Sealing Redistribution Layer Approach for Through-Glass via Fabrication. IEEE Journal of the Electron Devices Society, 2017, 5, 132-135.	2.1	6
84	Warpage Characteristics and Process Development of Through Silicon Via-Less Interconnection Technology. Journal of Nanoscience and Nanotechnology, 2018, 18, 5558-5565.	0.9	6
85	Ultra-High Strength Cu-Cu Bonding under Low Thermal Budget for Chiplet Heterogeneous Applications. , 2021, , .		6
86	Near-/Sub-V <inf>th</inf> process, voltage, and temperature (PVT) sensors with dynamic voltage selection. , 2013, , .		5
87	Area-power-efficient 11-bit SAR ADC with delay-line enhanced tuning for neural sensing applications. , 2013, , .		5
88	A TSV-Based Bio-Signal Package With \$mu\$-Probe Array. IEEE Electron Device Letters, 2014, 35, 256-258.	3.9	5
89	18.6 2.5D heterogeneously integrated bio-sensing microsystem for multi-channel neural-sensing applications. , 2014, , .		5
90	A Novel Flexible 3-D Heterogeneous Integration Scheme Using Electroless Plating on Chips With Advanced Technology Node. IEEE Transactions on Electron Devices, 2015, 62, 4148-4153.	3.0	5

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91	Ultrathin glass wafer lamination and laser debonding to enable glass interposer fabrication. , 2015, , .		5
92	Adhesion Property Between Cu, Ti Metal and SU-8, AZ 4620 Polymer Dielectric. Journal of Nanoscience and Nanotechnology, 2016, 16, 7546-7550.	0.9	5
93	Adhesion and Material Properties Between Polyimide and Passivation Layers for Polymer/Metal Hybrid Bonding in 3-D Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 412-418.	2.5	5
94	Investigation of Pillar–Concave Structure for Low-Temperature Cu–Cu Direct Bonding in 3-D/2.5-D Heterogeneous Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 1296-1303.	2.5	5
95	Enhanced growth of low-resistivity titanium silicides on epitaxial Si0.7Ge0.3 on (001)Si with a sacrificial amorphous Si interlayer. Thin Solid Films, 2010, 518, 7279-7282.	1.8	4
96	Bonding Temperature Optimization and Property Evolution of SU-8 Material in Metal/Adhesive Hybrid Wafer Bonding. Journal of Nanoscience and Nanotechnology, 2011, 11, 6969-6972.	0.9	4
97	3D heterogeneous integration structure based on 40 nm- and 0.18 ŵm-technology nodes. , 2015, , .		4
98	An ultra-high-density 256-channel/25mm2 neural sensing microsystem using TSV-embedded neural probes. , 2016, , .		4
99	Polymer for wafer-level hybrid bonding and its adhesion to passivation layer in 3D integration. , 2017, ,		4
100	Single-Crystal Islands (SCI) for Monolithic 3-D and Back-End-of-Line FinFET Circuits. IEEE Transactions on Electron Devices, 2021, 68, 5257-5262.	3.0	4
101	Study of Bondable Laser Release Material Using 355 nm Energy to Facilitate RDL-First and Die-First Fan-Out Wafer-Level Packaging (FOWLP). IEEE Transactions on Components, Packaging and Manufacturing Technology, 2022, 12, 692-699.	2.5	4
102	Investigation and Effects of Wafer Bow in 3D Integration Bonding Schemes. Journal of Electronic Materials, 2010, 39, 2605-2610.	2.2	3
103	The fabrication of a programmable via using phase-change material in CMOS-compatible technology. Nanotechnology, 2010, 21, 134001.	2.6	3
104	On-chip self-calibrated process-temperature sensor for TSV 3D integration. , 2012, , .		3
105	Low temperature bonding of Sn/In-Cu interconnects for three-dimensional integration applications. , 2013, , .		3
106	Quartz resonator assembling with TSV interposer using polymer sealing or metal bonding. Nanoscale Research Letters, 2014, 9, 541.	5.7	3
107	Interdiffusion of Cu-Sn system with Ni ultra-thin buffer layer and material analysis of IMC growth mechanism. , 2014, , .		3
108	Integrated microprobe array and CMOS MEMS by TSV technology for bio-signal recording application. , 2014, , .		3

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109	An ultra-fast temporary bonding and release process based on thin photolysis polymer in 3D integration. , 2015, , .		3
110	Wafer-level MOSFET with submicron photolysis polymer temporary bonding technology using ultra-fast laser ablation for 3DIC application. , 2016, , .		3
111	Investigation of Co Thin Film as Buffer Layer Applied to Cu/Sn Eutectic Bonding and UBM With Sn, SnCu, and SAC Solders Joints. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 7, 1899-1905.	2.5	3
112	Asymmetry hybrid bonding using Cu/Sn bonding with polyimide for 3D heterogeneous integration applications. , 2017, , .		3
113	Non-Planarization Cu-Cu Direct Bonding and Gang Bonding with Low Temperature and Short Duration in Ambient Atmosphere. , 2019, , .		3
114	Effect of Crystallinity on the Electrical Characteristics of Poly-Si Tunneling FETs via Green Nanosecond Laser Crystallization. IEEE Electron Device Letters, 2021, 42, 164-167.	3.9	3
115	Fabrication of Nano-Scale Cu Bond Pads with Seal Design in 3D Integration Applications. Journal of Nanoscience and Nanotechnology, 2011, 11, 3336-3339.	0.9	2
116	Electrical investigation and reliability of 3D integration platform using Cu TSVs and micro-bumps with Cu/Sn-BCB hybrid bonding. , 2013, , .		2
117	TSV-based quartz crystal resonator using 3D integration and Si packaging technologies. , 2013, , .		2
118	Low temperature (<180 °C) bonding for 3D integration. , 2013, , .		2
119	Energy-efficient configurable discrete wavelet transform for neural sensing applications. , 2014, , .		2
120	Investigation of low temperature Cu/In bonding in 3D integration. , 2015, , .		2
121	Device Characteristics of TSV-Based Piezoelectric Resonator With Load Capacitance and Static Capacitance Modification. IEEE Transactions on Electron Devices, 2015, 62, 927-933.	3.0	2
122	Study of a Novel Amorphous Silicon Temporary Bonding and Corresponding Laser Assisted De-bonding Technology. , 2016, , .		2
123	Development and electrical performance of low temperature Cu-Sn/In bonding for 3D flexible substate integration. , 2016, , .		2
124	The influence of device morphology on wafer-level bonding with polymer-coated layer. , 2016, , .		2
125	Study on low temperature Cu bonding and temporary bond/de-bond for RDL-first fan-out panel level package. , 2017, , .		2
126	Exploring the Correspondence Between Chemical States and Adhesion Property for Cr, Co Metal/AZ 4620, BCB Polymer Interface. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 195-201.	2.5	2

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127	Adhesion Property of Polyimide and Passivation Layer for Polymer/metal Wafer-Level Hybrid Bonding in 3D Integration. , 2018, , .		2
128	Low-Temperature Wafer-Level Metal Bonding with Gold Thin Film at 100 ŰC. , 2019, , .		2
129	Investigation of Low Temperature Cu Pillar Eutectic Bonding for 3D Chip Stacking Technology. , 2019, , $\cdot$		2
130	Versatile laser release material development for chip-first and chip-last fan-out wafer-level packaging. , 2021, , .		2
131	A hybrid bonding interconnection with a novel low-temperature bonding polymer system. , 2022, , .		2
132	Effects of Bonding Technology and Thinning Process in Three-Dimensional Integration on Device Characteristics. Journal of Nanoscience and Nanotechnology, 2012, 12, 8050-8054.	0.9	1
133	Multi-layer adaptive power management architecture for TSV 3DIC applications. , 2013, , .		1
134	Polymer TSV fabrication scheme with its electrical and reliability test vehicle. , 2014, , .		1
135	Low-temperature and low pressure copper-to-copper direct bonding enabled by creep on highly (111)-oriented Cu surfaces. , 2015, , .		1
136	Reliability investigation and mechanism analysis for a novel bonding method of flexible substrate in 3D integration. , 2016, , .		1
137	Electrical testing structure for stacking error measurement in 3D integration. , 2016, , .		1
138	An advanced 3D/2.5D integration packaging approach using double-self-assembly method with complex topography, and micropin-fin heat sink interposer for pressure sensing system. , 2016, , .		1
139	Fabrication of (111) nanotwinned Cu and its applications in interconnects of microelectronic devices. , 2016, , .		1
140	Feasibility Investigation of Amorphous Silicon as Release Layer in Temporary Bonding for 3-D Integration and FOWLP Scheme. IEEE Journal of the Electron Devices Society, 2017, 5, 136-140.	2.1	1
141	Development and electrical investigation of through glass via and through si via in 3D integration. , 2017, , .		1
142	Fine-Feature Cu/In Interconnect Bonding Using Single Sided Heating and Chip-to-Wafer Bonding Technology. IEEE Journal of the Electron Devices Society, 2017, 5, 128-131.	2.1	1
143	Breakthrough in Cu to Cu Pillar-Concave Bonding on Silicon Substrate with Polymer Layer for Advanced Packaging, 3D, and Heterogeneous Integration. , 2017, , .		1
144	Asymmetric Low Temperature Bonding Structure with Thin Solder Layers Using Ultra-Thin Buffer Layer. Journal of Nanoscience and Nanotechnology, 2018, 18, 5397-5403.	0.9	1

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145	Temperature Cycling Reliability of WOW Bumpless Through Silicon Vias. , 2019, , .		1
146	Adhesion Properties of Electroplating Process Between Polyimide and Metal Layer for Polymer/Metal Hybrid Bonding. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 168-175.	2.5	1
147	Evaluation of Metal/Polymer Adhesion and Highly Reliable Four-Point Bending Test Using Stealth Dicing Method in 3-D Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 956-962.	2.5	1
148	Investigation of Metal Interconnect for Wafer-Level and Sealable Miniaturized MEMS Encapsulation. IEEE Transactions on Electron Devices, 2021, , 1-5.	3.0	1
149	Investigation of Cu/In Thermosonic Bonding. Journal of Nanoscience and Nanotechnology, 2017, 17, 8890-8893.	0.9	1
150	Investigation of Low Temperature Co-Co Direct Bonding and Co-Passivated Cu-Cu Direct Bonding. , 2022, , .		1
151	Wafer-Level Self-Aligned Nano Tubular Structures and Templates for Device Applications. Journal of Nanoscience and Nanotechnology, 2010, 10, 8145-8150.	0.9	Ο
152	Micro-masking removal of TSV and cavity during ICP etching using parameter control in 3D and MEMS integrations. , 2012, , .		0
153	Investigation of ICP parameters for smooth tsvs and following cu plating process in 3D integration. , 2012, , .		Ο
154	Adhesive Selection and Bonding Parameter Optimization for Hybrid Bonding in 3D Integration. Journal of Nanoscience and Nanotechnology, 2012, 12, 1821-1828.	0.9	0
155	Co-sputtered Cu/Ti bonded interconnects for 3D integration applications. , 2013, , .		Ο
156	A TSV-based heterogeneous integrated neural-signal recording device with microprobe array. , 2014, , .		0
157	A novel Si-based X'tal oscillator device using 3D integration technologies. , 2014, , .		Ο
158	Research of electroplating and electroless plating for low temperature bonding in 3D heterogeneous integration. , 2014, , .		0
159	Advanced crystal component package with silicon TSV interposer using 3D integration and novel SU-8 polymer sealing bonding structure. , 2014, , .		Ο
160	Study of self-assembly technology for 3D integration applications. , 2015, , .		0
161	Electrical investigation of Cu pumping in through-silicon vias for BEOL reliability in 3D integration. , 2015, , .		0
162	Quality and reliability investigation of Ni/Sn transient liquid phase bonding technology. , 2015, , .		0

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163	High transmittance silicon terahertz polarizer using wafer bonding technology. Proceedings of SPIE, 2015, , .	0.8	Ο
164	Fabrication and reliability investigation of copper pillar and tapered through silicon via (TSV) for direct bonding in 3D integration. , 2015, , .		0
165	Single sided heating method for chip-to-wafer bonding with submicron Cu/In interconnects. , 2016, , .		Ο
166	Asymmetric low temperature bonding structure using ultra-thin buffer layer technique for 3D integration. , 2016, , .		0
167	Integration of neural sensing microsystem with TSV-embedded dissolvable µ-needles array, biocompatible flexible interposer, and neural recording circuits. , 2016, , .		0
168	High transmittance and broaden bandwidth through the morphology of anti-relfective layers on THz polarizer with Si substrate. Proceedings of SPIE, 2017, , .	0.8	0
169	A 64-channel wireless neural sensing microsystem with TSV-embedded micro-probe array for neural signal acquisition. , 2017, , .		0
170	High Transmittance Broadband THz Polarizer Using 3D-IC Technologies. , 2017, , .		0
171	Development and investigation of ultra-thin buffer layers used in symmetric Cu/Sn bonding and asymmetric Cu/Sn-Cu bonding for advanced 3D integration applications. , 2017, , .		0
172	Polymer-Based Liner TSV Fabrication Scheme and Its Resistance Variation. Journal of Nanoscience and Nanotechnology, 2017, 17, 4712-4715.	0.9	0
173	Uneven-Topography-Chip Packing Approach Using Double-Self-Assembly Technology for 3-D Heterogeneous Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 310-316.	2.5	0
174	Low Temperature Bonding Technology Development for 3D and Heterogeneous Integration. , 2018, , .		0
175	Simulation Analysis of Structure Design for Low Temperature Cu-Cu Direct Bonding in Heterogeneous Integration and Advanced Packaging Systems. , 2018, , .		Ο
176	A Novel Method of Electrical Measurement for Stacking Error in 3D/2.5D Integration. Journal of Nanoscience and Nanotechnology, 2018, 18, 1066-1069.	0.9	0
177	A Design Flow for Micro Bump and Stripe Planning on Modern Chip-Package Co-Design. , 2020, , .		0
178	Advanced 2.5D Heterogeneous Integrated Platform Using Flexible Biocompatible Substrate for Biomedical Sensing System. , 2021, , .		0
179	Low Temperature Cu-Cu Bonding with Electroless Deposited Metal Passivation for Fine-Pitch 3D Packaging. , 2021, , .		0
180	3D Integration Scheme Demonstration Using Wafer Bonding. , 2019, , 209-223.		0

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181	Polymer Adhesive Bonding. , 2019, , 1-13.		0
182	Crystal Resonator Application. , 2019, , 225-254.		0
183	Cu–Cu Direct Bonding. , 2019, , 65-80.		0
184	Cu, Sn, and In Low Temperature Bonding. , 2019, , 129-147.		0
185	Metal Bonding: Introduction and Non-Cu-Based. , 2019, , 51-64.		0
186	Hybrid Metal/Dielectric Bonding. , 2019, , 199-208.		0
187	RF Characterization on Nb-based Superconducting Silicon Interconnect Fabric for Future Large Scale Quantum Applications. , 2022, , .		0