Naoya Watanabe

List of Publications by Year
in descending order

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Version: 2024-02-01

		1040056	1199594
31	202	9	12
papers	citations	h-index	g-index

31	31	31	179
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices. IEEE Journal of Solid-State Circuits, 2020, 55, 2747-2755.	5.4	17
2	3-D CMOS Chip Stacking for Security ICs Featuring Backside Buried Metal Power Delivery Networks With Distributed Capacitance. IEEE Transactions on Electron Devices, 2021, 68, 2077-2082.	3.0	14
3	Validation of TSV thermo-mechanical simulation by stress measurement. Microelectronics Reliability, 2016, 59, 95-101.	1.7	13
4	Fabrication and stress analysis of annular-trench-isolated TSV. Microelectronics Reliability, 2016, 63, 142-147.	1.7	12
5	A Thick Cu Layer Buried in Si Interposer Backside for Global Power Routing. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 502-510.	2.5	11
6	Fully epitaxial giant magnetoresistive devices with half-metallic Heusler alloy fabricated on poly-crystalline electrode using three-dimensional integration technology. Acta Materialia, 2020, 200, 1038-1045.	7.9	11
7	Fabrication and electrical characterization of Parylene-HT liner bottom-up copper filled through silicon via (TSV). , 2014, , .		10
8	15-Âµm-pitch Cu/Au interconnections relied on self-aligned low-temperature thermosonic flip-chip bonding technique for advanced chip stacking applications. Japanese Journal of Applied Physics, 2014, 53, 04EB04.	1.5	10
9	Three-dimensional integration technology of magnetic tunnel junctions for magnetoresistive random access memory application. Applied Physics Express, 2017, 10, 063002.	2.4	10
10	Development of a high-yield via-last through silicon via process using notchless silicon etching and wet cleaning of the first metal layer. Japanese Journal of Applied Physics, 2017, 56, 07KE02.	1.5	10
11	Copper-Filled Through-Silicon Vias With Parylene-HT Liner. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 510-517.	2.5	9
12	Residual stress investigation of via-last through-silicon via by polarized Raman spectroscopy measurement and finite element simulation. Japanese Journal of Applied Physics, 2018, 57, 07MF02.	1.5	9
13	Stress investigation of annular-trench-isolated TSV by polarized Raman spectroscopy measurement and finite element simulation. Microelectronics Reliability, 2019, 99, 125-131.	1.7	8
14	Novel through silicon via exposure process comprising Si/Cu grinding, electroless Niâ€"B plating, and wet etching of Si. Japanese Journal of Applied Physics, 2014, 53, 05GE02.	1.5	7
15	Damage Evaluation of Wet-Chemical Si-Wafer Thinning/Backside Via Exposure Process. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 741-747.	2.5	7
16	Modified thermosonic flip-chip bonding based on electroplated Cu microbumps and concave pads for high-precision low-temperature assembly applications. , 2013, , .		6
17	Development of a chip prober for pre-bond testing of a 3D-IC. , 2013, , .		5
18	A Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices. , 2019, , .		5

#	Article	IF	Citations
19	New optical three dimensional structure measurement method of cone shape micro bumps used for 3D LSI chip stacking. , 2013, , .		4
20	Fabrication of a membrane probe card using transparent film for three-dimensional integrated circuit testing. Japanese Journal of Applied Physics, 2014, 53, 06JM06.	1.5	4
21	Small-diameter TSV reveal process using direct Si/Cu grinding and metal contamination removal. , 2014, , .		4
22	Thermal Stress Comparison of Annular-Trench-Isolated (ATI) TSV with Cu and Solder Core. , 2019, , .		3
23	Material effect on thermal stress of annular-trench-isolated through silicon via (TSV). Japanese Journal of Applied Physics, 2020, 59, SLLH01.	1.5	3
24	3D IC testing using a chip prober and a transparent membrane probe card. , 2014, , .		2
25	Impact of thinning stacked dies on the thermal resistance of bump-bonded three-dimensional integrated circuits. Microelectronics Reliability, 2016, 67, 2-8.	1.7	2
26	Over-the-top Si Interposer Embedding Backside Buried Metal PDN to Reduce Power Supply Impedance of Large Scale Digital ICs. , 2019, , .		2
27	High-speed optical three dimensional measurement method for micro bump inspection in 3D LSI chip stacking technology. , 2015, , .		1
28	Thermal impact of extreme die thinning in bump-bonded three-dimensional integrated circuits. Microelectronics Reliability, 2017, 79, 380-386.	1.7	1
29	Fabrication and stacking of through-silicon-via array chip formed by notchless Si etching and wet cleaning of first metal layer. Japanese Journal of Applied Physics, 2019, 58, SDDL09.	1.5	1
30	Investigation of metal contamination induced by a through silicon via reveal process using direct Si/Cu grinding and residual metal removal. Japanese Journal of Applied Physics, 2016, 55, 06GP06.	1.5	1
31	Development of Three-Dimensional Integration Technology for Magnetic Random Access Memories. Journal of Japan Institute of Electronics Packaging, 2019, 22, 495-500.	0.1	0