

Yajun Ha

List of Publications by Year in descending order

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| # | ARTICLE | IF | CITATIONS |
|----|--|-----|-----------|
| 1 | Interference-Minimized Multipath Routing with Congestion Control in Wireless Sensor Network for High-Rate Streaming. IEEE Transactions on Mobile Computing, 2008, 7, 1124-1137. | 3.9 | 138 |
| 2 | An Ultra-Low-Energy Multi-Standard JPEG Co-Processor in 65 nm CMOS With Sub/Near Threshold Supply Voltage. IEEE Journal of Solid-State Circuits, 2010, 45, 668-680. | 3.5 | 73 |
| 3 | FPGA-Based 40.9-Gbits/s Masked AES With Area Optimization for Storage Area Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 36-40. | 2.2 | 69 |
| 4 | A Low Active Leakage and High Reliability Phase Change Memory (PCM) Based Non-Volatile FPGA Storage Element. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2605-2613. | 3.5 | 65 |
| 5 | Improved chaff point generation for vault scheme in bio-cryptosystems. IET Biometrics, 2013, 2, 48-55. | 1.6 | 62 |
| 6 | A 65-nm 25.1-ns 30.7-fJ Robust Subthreshold Level Shifter With Wide Conversion Range. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 671-675. | 2.2 | 49 |
| 7 | Generalized Hyperbolic CORDIC and Its Logarithmic and Exponential Computation With Arbitrary Fixed Base. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2156-2169. | 2.1 | 34 |
| 8 | PLAC: Piecewise Linear Approximation Computation for All Nonlinear Unary Functions. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2014-2027. | 2.1 | 32 |
| 9 | A Universal Method of Linear Approximation With Controllable Error for the Efficient Implementation of Transcendental Functions. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 177-188. | 3.5 | 31 |
| 10 | Analyzing composability of applications on MPSoC platforms. Journal of Systems Architecture, 2008, 54, 369-383. | 2.5 | 29 |
| 11 | Pseudo-random single photon counting for time-resolved optical measurement. Optics Express, 2008, 16, 13233. | 1.7 | 26 |
| 12 | Analysis and Optimization Strategies Toward Reliable and High-Speed 6T Compute SRAM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1520-1531. | 3.5 | 23 |
| 13 | Quality-Driven Dynamic Scheduling for Real-Time Adaptive Applications on Multiprocessor Systems. IEEE Transactions on Computers, 2013, 62, 2026-2040. | 2.4 | 22 |
| 14 | An energy-efficient system on a programmable chip platform for cloud applications. Journal of Systems Architecture, 2017, 76, 117-132. | 2.5 | 20 |
| 15 | Efficient FPGA Implementation of K-Nearest-Neighbor Search Algorithm for 3D LIDAR Localization and Mapping in Smart Vehicles. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1644-1648. | 2.2 | 16 |
| 16 | Iterative Probabilistic Performance Prediction for Multi-Application Multiprocessor Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 538-551. | 1.9 | 15 |
| 17 | Performance and security-enhanced fuzzy vault scheme based on ridge features for distorted fingerprints. IET Biometrics, 2015, 4, 29-39. | 1.6 | 15 |
| 18 | Mapping real-life applications on run-time reconfigurable NoC-based MPSoC on FPGA. , 2010, , . | | 14 |

| # | ARTICLE | IF | CITATIONS |
|----|---|-----|-----------|
| 19 | An area-efficient dynamically reconfigurable Spatial Division Multiplexing network-on-chip with static throughput guarantee. , 2010, , . | | 14 |
| 20 | An FPGA-Based Cloud System for Massive ECG Data Analysis. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 309-313. | 2.2 | 14 |
| 21 | A 55nm, 0.4V 5526-TOPS/W Compute-in-Memory Binarized CNN Accelerator for AIoT Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1695-1699. | 2.2 | 14 |
| 22 | Building a Virtual Framework for Networked Reconfigurable Hardware and Software Objects. Journal of Supercomputing, 2002, 21, 131-144. | 2.4 | 12 |
| 23 | A directional coarse-grained power gated FPGA switch box and power gating aware routing algorithm. , 2013, , . | | 12 |
| 24 | Reconfiguring Three-Dimensional Processor Arrays for Fault-Tolerance: Hardness and Heuristic Algorithms. IEEE Transactions on Computers, 2015, 64, 2926-2939. | 2.4 | 12 |
| 25 | A Reliable 8T SRAM for High-Speed Searching and Logic-in-Memory Operations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 769-780. | 2.1 | 12 |
| 26 | A 0.4V 280-nW frequency reference-less nearly all-digital hybrid domain temperature sensor. , 2014, , . | | 11 |
| 27 | Dynamic Scheduling of Imprecise-Computation Tasks on Real-Time Embedded Multiprocessors. , 2013, , . | | 10 |
| 28 | Analysis and Design of Reconfigurable Sense Amplifier for Compute SRAM With High-Speed Compute and Normal Read Access. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3503-3507. | 2.2 | 10 |
| 29 | An Optimized Logarithmic Converter With Equal Distribution of Relative Errors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 848-852. | 2.2 | 9 |
| 30 | Hierarchical topometric representation of 3D robotic maps. Autonomous Robots, 2021, 45, 755-771. | 3.2 | 9 |
| 31 | Optimizing energy efficiency of CNN-based object detection with dynamic voltage and frequency scaling. Journal of Semiconductors, 2020, 41, 022406. | 2.0 | 8 |
| 32 | An Optimized FPGA-Based Real-Time NDT for 3D-LiDAR Localization in Smart Vehicles. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3167-3171. | 2.2 | 8 |
| 33 | Quality Optimization of Resilient Applications under Temperature Constraints. , 2017, , . | | 7 |
| 34 | Vulnerability of Deep Learning Model based Anomaly Detection in Vehicle Network. , 2020, , . | | 7 |
| 35 | DVFS-Based Scrubbing Scheduling for Reliability Maximization on Parallel Tasks in SRAM-based FPGAs. , 2020, , . | | 7 |
| 36 | Correlation ratio based volume image registration on GPUs. Microprocessors and Microsystems, 2015, 39, 998-1011. | 1.8 | 6 |

| # | ARTICLE | IF | CITATIONS |
|----|--|-----|-----------|
| 37 | A New CMOS Buffer Amplifier Design Used in Low Voltage MEMS Interface Circuits. Analog Integrated Circuits and Signal Processing, 2001, 27, 7-17. | 0.9 | 5 |
| 38 | An Area-Efficient Timing-Driven Routing Algorithm for Scalable FPGAs with Time-Multiplexed Interconnects. , 2008, , . | | 5 |
| 39 | A Hardware Pipeline with High Energy and Resource Efficiency for FMM Acceleration. Transactions on Embedded Computing Systems, 2018, 17, 1-20. | 2.1 | 5 |
| 40 | Energy-Efficient Arbitrary Precision Multi-Bit Multiplication with Bi-Serial In/Near Memory Computing. , 2020, , . | | 5 |
| 41 | Quality Estimation and Optimization of Adaptive Stereo Matching Algorithms for Smart Vehicles. Transactions on Embedded Computing Systems, 2020, 19, 1-24. | 2.1 | 5 |
| 42 | FPGA Accelerator for Real-Time Non-Line-of-Sight Imaging. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 721-734. | 3.5 | 5 |
| 43 | Interference-Minimized Multipath Routing with Congestion Control in Wireless Sensor Network for Multimedia Streaming. , 2007, , . | | 4 |
| 44 | ParaLaR: A parallel FPGA router based on Lagrangian relaxation. , 2015, , . | | 4 |
| 45 | Enabling Fine-Grained Dynamic Voltage and Frequency Scaling in SDSoC. , 2019, , . | | 4 |
| 46 | Energy Efficiency Optimization of FPGA-based CNN Accelerators with Full Data Reuse and VFS. , 2019, , . | | 4 |
| 47 | FODM: A Framework for Accurate Online Delay Measurement Supporting All Timing Paths in FPGA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 502-514. | 2.1 | 4 |
| 48 | Providing both guaranteed and best effort services using Spatial Division Multiplexing NoC with dynamic channel allocation and runtime reconfiguration. , 2008, , . | | 3 |
| 49 | An area-efficient shuffling scheme for AES implementation on FPGA. , 2013, , . | | 3 |
| 50 | DVFS-Based Quality Maximization for Adaptive Applications With Diminishing Return. IEEE Transactions on Computers, 2021, 70, 803-816. | 2.4 | 3 |
| 51 | Quality Optimization of Adaptive Applications via Deep Reinforcement Learning in Energy Harvesting Edge Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4873-4886. | 1.9 | 3 |
| 52 | Robustness-driven energy-efficient ultra-low voltage standard cell design with intra-cell mixed-V<inf>t</inf> methodology. , 2013, , . | | 2 |
| 53 | TRISHUL: A single-pass optimal two-level inclusive data cache hierarchy selection process for real-time MPSoCs. , 2013, , . | | 2 |
| 54 | FPGA based Rekeying for cryptographic key management in Storage Area Network. , 2013, , . | | 2 |

| # | ARTICLE | IF | CITATIONS |
|----|---|-----|-----------|
| 55 | Corrections to "Generalized Hyperbolic CORDIC and Its Logarithmic and Exponential Computation With Arbitrary Fixed Base" [Sep 19 DOI: 10.1109/TVLSI.2019.2919557]. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2222-2222. | 2.1 | 2 |
| 56 | An automated, efficient and static bit-width optimization methodology towards maximum bit-width-to-error tradeoff with affine arithmetic model. , 0, , . | | 1 |
| 57 | Dynamic scheduling of imprecise-computation tasks in maximizing QoS under energy constraints for embedded systems. , 2008, , . | | 1 |
| 58 | sFPGA — A scalable switch based FPGA architecture and design methodology. , 2008, , . | | 1 |
| 59 | A low overhead fault tolerant FPGA with new connection box. , 2008, , . | | 1 |
| 60 | An optimized design for serial-parallel finite field multiplication over $GF(2^m)$ based on all-one polynomials. , 2009, , . | | 1 |
| 61 | Area Efficient Box Filter Acceleration by Parallelizing with Optimized Adder Tree. , 2019, , . | | 1 |
| 62 | CLIF: Cross-Layer Information Fusion for Stereo Matching and its Hardware Implementation. , 2021, , . | | 1 |
| 63 | Bitwidth-Optimized Energy-Efficient FFT Design via Scaling Information Propagation. , 2021, , . | | 1 |
| 64 | Ultra-Fast FPGA Implementation of Graph Cut Algorithm With Ripple Push and Early Termination. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1532-1545. | 3.5 | 1 |
| 65 | Tighter WCET analysis of input dependent programs with classified-cache memory architecture. , 2008, , . | | 0 |
| 66 | An architecture and timing-driven routing algorithm for area-efficient FPGAs with time-multiplexed interconnects. , 2008, , . | | 0 |
| 67 | sFPGA2 - A scalable GALS FPGA architecture and design methodology. , 2009, , . | | 0 |
| 68 | B*-tree based variability-aware floorplanning. , 2010, , . | | 0 |
| 69 | A Hilbert curve-based delay fault characterization method for FPGAs. , 2011, , . | | 0 |
| 70 | The architecture and placement algorithm for a uni-directional routing based 3D FPGA. , 2013, , . | | 0 |
| 71 | Analysis and design of energy-efficient data-dependent SRAM. , 2017, , . | | 0 |
| 72 | AxC-CS: Approximate Computing for Hardware Efficient Compressed Sensing Encoder Design. , 2019, , . | | 0 |

| # | ARTICLE | IF | CITATIONS |
|----|--|-----|-----------|
| 73 | Guest Editorial Special Issue on the 2020 ISICAS: A CAS Journal Track Symposium. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1493-1493. | 2.2 | 0 |
| 74 | Guest Editorial Special Issue on the 2020 IEEE International Symposium on Circuits and Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 805-805. | 2.2 | 0 |
| 75 | Guest Editorial Special Issue on the 2021 IEEE International Symposium on Circuits and Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1565-1565. | 2.2 | 0 |
| 76 | Guest Editorial Special Issue on the 2021 ISICAS: A CAS Journal Track Symposium. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3037-3037. | 2.2 | 0 |
| 77 | Incoming Editorial. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2-4. | 2.2 | 0 |