Ioannis Savidis

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/9206708/publications.pdf

Version: 2024-02-01

49 papers	715 citations	1040056 9 h-index	888059 17 g-index
49 all docs	49 docs citations	49 times ranked	495 citing authors

#	Article	IF	Citations
1	Adaptive-Gravity: A Defense Against Adversarial Samples. , 2022, , .		0
2	Increased Output Corruption and Structural Attack Resilience for SAT Attack Secure Logic Locking. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 38-51.	2.7	6
3	Synthesis of Hidden State Transitions for Sequential Logic Locking. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 11-23.	2.7	8
4	SAT-attack Resilience Measure for Access Restricted Circuits. , 2021, , .		0
5	Performance and Security Analysis of Parameter-Obfuscated Analog Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 2013-2026.	3.1	9
6	Leakage Reuse for Energy Efficient Near-Memory Computing of Heterogeneous DNN Accelerators. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 762-775.	3.6	1
7	Characterization of In-Cone Logic Locking Resiliency Against the SAT Attack. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1607-1620.	2.7	7
8	Recycling of unused leakage current for energy efficient multi-voltage systems. Microelectronics Journal, 2020, 101, 104782.	2.0	2
9	Modeling SAT-Attack Search Complexity. , 2020, , .		1
10	Dynamic idle core management and leakage current reuse in MPSoC platforms. , 2020, , .		2
11	Mesh Based Obfuscation of Analog Circuit Properties. , 2019, , .		14
12	Reusing Leakage Current for Improved Energy Efficiency of Multi-Voltage Systems. , 2019, , .		2
13	Securing Analog Mixed-Signal Integrated Circuits Through Shared Dependencies. , 2019, , .		11
14	Evolving On-Chip Power Delivery through Particle Swarm Optimization. , 2019, , .		0
15	Applying Swarm Intelligence to Distributed On-Chip Power Management. , 2019, , .		0
16	Power conversion efficiency-aware mapping of multithreaded applications on heterogeneous architectures: A comprehensive parameter tuning. , 2018, , .		5
17	ElasticCore: A Dynamic Heterogeneous Platform With Joint Core and Voltage/Frequency Scaling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 249-261.	3.1	3
18	Transistor Sizing for Parameter Obfuscation of Analog Circuits Using Satisfiability Modulo Theory. , 2018, , .		3

#	Article	IF	Citations
19	Multi-Voltage Domain Power Distribution Network for Optimized Ultra-Low Voltage Clock Delivery. , 2018, , .		1
20	Importance of Multi-parameter SAT Attack Exploration for Integrated Circuit Security. , 2018, , .		4
21	Noise Constrained Optimum Selection of Supply Voltage for IoT Applications. , 2018, , .		2
22	Time Domain Sequential Locking for Increased Security. , 2018, , .		13
23	On-Chip Power Supply Noise Suppression Through Hyperabrupt Junction Varactors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2230-2240.	3.1	4
24	Protecting analog circuits with parameter biasing obfuscation. , 2017, , .		28
25	Smart Grid on Chip: Work Load-Balanced On-Chip Power Delivery. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2538-2551.	3.1	10
26	Clock tree synthesis for heterogeneous 3-D integrated circuits. , 2017, , .		0
27	Bi-directional input/output circuits with integrated level shifters for near-threshold computing. , 2017, , .		4
28	A framework for exploring alternative fault-tolerant schemes targeting 3-D reconfigurable architectures. , 2016, , .		1
29	Heterogeneous 3-D circuits: Integrating free-space optics with CMOS. Microelectronics Journal, 2016, 50, 66-75.	2.0	8
30	Reducing logic encryption overhead through gate level key insertion. , 2016, , .		22
31	Robust near-threshold inverter with improved performance for ultra-low power applications. , 2016, , .		3
32	Energy efficient on-chip power delivery with run-time voltage regulator clustering. , 2016, , .		6
33	Reduced Overhead Gate Level Logic Encryption. , 2016, , .		23
34	Realizing complexity-effective on-chip power delivery for many-core platforms by exploiting optimized mapping. , 2015, , .		7
35	Experimental Analysis of Thermal Coupling in 3-D Integrated Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2077-2089.	3.1	9
36	ElasticCore. , 2015, , .		18

#	Article	IF	Citations
37	Thermal conduction path analysis in 3-D ICs. , 2014, , .		9
38	Run-time voltage detection circuit for 3-D IC power delivery. , 2014, , .		1
39	Power Noise in TSV-Based 3-D Integrated Circuits. IEEE Journal of Solid-State Circuits, 2013, 48, 587-597.	5.4	18
40	3-D integrated heterogeneous intra-chip free-space optical interconnect. Optics Express, 2012, 20, 4331.	3.4	46
41	Clock Distribution Networks in 3-D Integrated Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 2256-2266.	3.1	38
42	Clock distribution models of 3-D integrated systems. , 2011, , .		1
43	A 3-D Integrated Intrachip Free-Space Optical Interconnect for Many-Core Chips. IEEE Photonics Technology Letters, 2011, 23, 164-166.	2.5	22
44	Thermal analysis of oxide-confined VCSEL arrays. Microelectronics Journal, 2011, 42, 820-825.	2.0	29
45	An intra-chip free-space optical interconnect. , 2010, , .		45
46	Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance. IEEE Transactions on Electron Devices, 2009, 56, 1873-1881.	3.0	179
47	Electrical modeling and characterization of 3-D vias. , 2008, , .		50
48	Clock distribution networks for 3-D ictegrated Circuits. , 2008, , .		36
49	Clock distribution architectures for 3-D SOI integrated circuits. , 2008, , .		4