Khyamling Parane

List of Publications by Year
in descending order

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15 papers	45 citations	2258059 3 h-index	2053705 5 g-index

15 all docs	15 docs citations	15 times ranked	25 citing authors

#	Article	IF	Citations
1	Internet-of-things and mobile application based hybrid model for controlling energy system. International Journal of Information Technology (Singapore), 2021, 13, 2129.	2.7	3
2	FPGA friendly NoC simulation acceleration framework employing the hard blocks. Computing (Vienna/New York), 2021, 103, 1791.	4.8	6
3	Hy-BTree: An efficient Tree based topology for FPGA based NoC implementation. , 2021, , .		1
4	An Efficient FPGA-Based Network-on-Chip Simulation Framework Utilizing the Hard Blocks. Circuits, Systems, and Signal Processing, 2020, 39, 5247-5271.	2.0	6
5	P-NoC: Performance Evaluation and Design Space Exploration of NoCs for Chip Multiprocessor Architecture Using FPGA. Wireless Personal Communications, 2020, 114, 3295-3319.	2.7	3
6	LBNoC. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-26.	2.6	6
7	Design of an Adaptive and Reliable Network on Chip Router Architecture Using FPGA. , 2019, , .		4
8	High-Performance NoC Simulation Acceleration Framework Employing the Xilinx DSP48E1 Blocks. , 2019, , .		2
9	Analysis of cache behaviour and software optimizations for faster on-chip network simulations. International Journal of Systems Assurance Engineering and Management, 2019, 10, 696-712.	2.4	0
10	High-Performance NoCs Employing the DSP48E1 Blocks of the Xilinx FPGAs. , 2019, , .		1
11	YaNoC: Yet Another Network-on-Chip Simulation Acceleration Engine Supporting Congestion-Aware Adaptive Routing Using FPGAs. Journal of Circuits, Systems and Computers, 2019, 28, 1950202.	1.5	2
12	Trace-Driven Simulation and Design Space Exploration of Network-on-Chip Topologies on FPGA. , 2018, , .		3
13	FPGA based NoC Simulation Acceleration Framework Supporting Adaptive Routing. , 2018, , .		4
14	YaNoC: Yet Another Network-on-Chip Simulation Acceleration Engine Using FPGAs. , 2018, , .		4
15	Cache analysis and software optimizations for faster on-chip network simulations. , 2016, , .		0