

# F Eugenio Potestad-OrdÃ³ñez

## List of Publications by Year in descending order

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Version: 2024-02-01

13  
papers

46  
citations

2258059

3  
h-index

2053705

5  
g-index

13  
all docs

13  
docs citations

13  
times ranked

22  
citing authors

#	ARTICLE	IF	CITATIONS
1	Hardware Countermeasures Benchmarking against Fault Attacks. Applied Sciences (Switzerland), 2022, 12, 2443.	2.5	4
2	Gate-Level Hardware Countermeasure Comparison against Power Analysis Attacks. Applied Sciences (Switzerland), 2022, 12, 2390.	2.5	3
3	Design and Evaluation of Countermeasures Against Fault Injection Attacks and Power Side-Channel Leakage Exploration for AES Block Cipher. IEEE Access, 2022, 10, 65548-65561.	4.2	5
4	Experimental FIA Methodology Using Clock and Control Signal Modifications under Power Supply and Temperature Variations. Sensors, 2021, 21, 7596.	3.8	0
5	Trivium Stream Cipher Countermeasures Against Fault Injection Attacks and DFA. IEEE Access, 2021, 9, 168444-168454.	4.2	1
6	An Academic Approach to FPGA Design Based on a Distance Meter Circuit. Revista Iberoamericana De Tecnologías Del Aprendizaje, 2020, 15, 123-128.	0.9	0
7	Breaking Trivium Stream Cipher Implemented in ASIC Using Experimental Attacks and DFA. Sensors, 2020, 20, 6909.	3.8	5
8	FPGA design example for maximum operating frequency measurements. , 2018, , .		0
9	Distance measurement as a practical example of FPGA design. , 2018, , .		1
10	Floorplanning as a practical countermeasure against clock fault attack in Trivium stream cipher. , 2018, , .		1
11	Vulnerability Analysis of Trivium FPGA Implementations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3380-3389.	3.1	17
12	Experimental and timing analysis comparison of FPGA trivium implementations and their vulnerability to clock fault injection. , 2016, , .		2
13	Fault attack on FPGA implementations of Trivium stream cipher. , 2016, , .		7