Srinivasan Gopal

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/9125086/publications.pdf

Version: 2024-02-01

20 papers	234 citations	1307594 7 h-index	1588992 8 g-index
20 all docs	20 docs citations	20 times ranked	223 citing authors

#	Article	IF	Citations
1	A 28GHz 41%-PAE linear CMOS power amplifier using a transformer-based AM-PM distortion-correction technique for 5G phased arrays. , 2018, , .		54
2	A 25â€“35 GHz Neutralized Continuous Class-F CMOS Power Amplifier for 5G Mobile Communications Achieving 26% Modulation PAE at 1.5 Gb/s and 46.4% Peak PAE. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 834-847.	5.4	40
3	Transformer-Based Predistortion Linearizer for High Linearity and High Modulation Efficiency in mm-Wave 5G CMOS Power Amplifiers. IEEE Transactions on Microwave Theory and Techniques, 2019, 67, 3074-3087.	4.6	23
4	A Continually-Stepped Variable-Gain LNA in 65-nm CMOS Enabled by a Tunable-Transformer for mm-Wave 5G Communications. , 2019, , .		19
5	Current reuse triple-band signal source for multi-band wireless network-on-chip. , 2017, , .		11
6	A Spatial Multi-Bit Sub-1-V Time-Domain Matrix Multiplier Interface for Approximate Computing in 65-nm CMOS. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 506-518.	3.6	11
7	Energy and Area Efficient Near Field Inductive Coupling. , 2017, , .		10
8	High-Performance and Small-Form Factor Near-Field Inductive Coupling for 3-D NoC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2921-2934.	3.1	9
9	A 16-Gb/s Low-Power Inductorless Wideband Gain-Boosted Baseband Amplifier With Skewed Differential Topology for Wireless Network-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2406-2418.	3.1	9
10	A Highly Efficient Dual-band Harmonic-tuned GaN RF Synchronous Rectifier with Integrated Coupler and Phase Shifter. , 2019, , .		8
11	Analysis of Systematic Losses in Hybrid Envelope Tracking Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1319-1330.	5.4	8
12	A Hybrid 3D Interconnect With 2x Bandwidth Density Employing Orthogonal Simultaneous Bidirectional Signaling for 3D NoC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3919-3932.	5.4	7
13	Making a Case for Partially Connected 3D NoC. ACM Journal on Emerging Technologies in Computing Systems, 2020, 16, 1-17.	2.3	6
14	An Echo-Canceller-less NFIC- TSV Hybrid 3D Interconnect for Simultaneous Bidirectional Vertical Communication. , 2018, , .		4
15	A Low Power Active-Passive Dual Gm-boosted W-band Oscillator for Wireless Networ -on-Chip Applications. , 2018, , .		4
16	Energy-efficient and robust 3D NoCs with contactless vertical links (Invited paper). , 2017, , .		3
17	Dual-Equalization-Path Energy-Area-Efficient Near Field Inductive Coupling for Contactless 3D IC. , 2019, , .		3
18	Trends and Opportunities for SRAM Based In-Memory and Near-Memory Computation. , 2021, , .		3

#	Article	IF	Citations
19	Hierarchical Design Methodology and Optimization for Proximity Communication based Contactless 3D ThruChip Interface. , 2019, , .		1
20	A Reconfigurable Asynchronous SERDES for Heterogenous Chiplet Interconnects. , 2021, , .		1