Tomohiro Korikawa

List of Publications by Year
in descending order

7	24	2682572 2	2550090 3
papers	citations	h-index	g-index

7	7	7	7
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Packet Processing Architecture with Off-Chip Last Level Cache Using Interleaved 3D-Stacked DRAM. IEICE Transactions on Communications, 2021, E104.B, 149-157.	0.7	1
2	Memory Network Architecture for Packet Processing in Functions Virtualization. , 2021, , .		1
3	Packet Processing Architecture Using Last-Level-Cache Slices and Interleaved 3D-Stacked DRAM. IEEE Access, 2020, 8, 59290-59304.	4.2	4
4	Carrier-Scale Packet Processing Architecture Using Interleaved 3D-Stacked DRAM and Its Analysis. IEEE Access, 2019, 7, 75500-75514.	4.2	6
5	Packet Processing Architecture With Off-Chip LLC Using Interleaved 3D-Stacked DRAM. , 2019, , .		3
6	Carrier-Scale Packet Processing System Using Interleaved 3D-Stacked DRAM. , 2018, , .		7
7	Toward carrier-scale general-purpose node. , 2017, , .		2