## Tomohiro Korikawa

List of Publications by Year in descending order

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2682572 2550090 7 24 2 3 citations g-index h-index papers 7 7 7 7 citing authors docs citations times ranked all docs

#	Article	IF	CITATIONS
1	Carrier-Scale Packet Processing System Using Interleaved 3D-Stacked DRAM. , 2018, , .		7
2	Carrier-Scale Packet Processing Architecture Using Interleaved 3D-Stacked DRAM and Its Analysis. IEEE Access, 2019, 7, 75500-75514.	4.2	6
3	Packet Processing Architecture Using Last-Level-Cache Slices and Interleaved 3D-Stacked DRAM. IEEE Access, 2020, 8, 59290-59304.	4.2	4
4	Packet Processing Architecture With Off-Chip LLC Using Interleaved 3D-Stacked DRAM., 2019, , .		3
5	Toward carrier-scale general-purpose node. , 2017, , .		2
6	Packet Processing Architecture with Off-Chip Last Level Cache Using Interleaved 3D-Stacked DRAM. IEICE Transactions on Communications, 2021, E104.B, 149-157.	0.7	1
7	Memory Network Architecture for Packet Processing in Functions Virtualization. , 2021, , .		1