Chan Shan

List of Publications by Year in descending order

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		1684188	1372567	
11	126	5	10	
papers	citations	h-index	g-index	
12	12	12	131	
all docs	docs citations	times ranked	citing authors	

#	Article	IF	CITATIONS
1	In-Built N+ Pocket Electrically Doped Tunnel FET With Improved DC and Analog/RF Performance. Micromachines, 2020, 11, 960.	2.9	5
2	3D Numerical Simulation of a Z Gate Layout MOSFET for Radiation Tolerance. Micromachines, 2018, 9, 659.	2.9	9
3	Negative bias temperature instability in SOIâ€like pâ€type metal oxide semiconductor devices. Micro and Nano Letters, 2018, 13, 1151-1154.	1.3	0
4	Reliability improvements in SOIâ€like MOSFET with ESD and selfâ€heating effect. Micro and Nano Letters, 2018, 13, 1649-1652.	1.3	4
5	A high-performance channel engineered charge-plasma-based MOSFET with high- $\hat{\mathbb{I}}^2$ spacer. Superlattices and Microstructures, 2017, 112, 499-506.	3.1	4
6	A Low Turn-Off Loss 4H-SiC Trench IGBT With Schottky Contact in the Collector Side. IEEE Transactions on Electron Devices, 2017, 64, 4575-4580.	3.0	13
7	Graded-channel junctionless dual-gate MOSFETs for radiation tolerance. Japanese Journal of Applied Physics, 2017, 56, 124201.	1.5	5
8	A Charge-Plasma-Based Transistor With Induced Graded Channel for Enhanced Analog Performance. IEEE Transactions on Electron Devices, 2016, 63, 2275-2281.	3.0	47
9	Improved performance of nanoscale junctionless transistor based on gate engineering approach. Microelectronics Reliability, 2015, 55, 318-325.	1.7	27
10	A Simulation Study of Hot Carrier Effects in Sol-Like Bulk Silicon nMOS Device. IEEE Transactions on Electron Devices, 2015, 62, 23-27.	3.0	5
11	A Simulation Study of Sol-Like Bulk Silicon MOSFET With Improved Performance. IEEE Transactions on Electron Devices, 2014, 61, 3339-3344.	3.0	7