

# Chan Shan

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/9122964/publications.pdf>

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papers

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1683934

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1372474

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docs citations

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131  
citing authors

#	ARTICLE	IF	CITATIONS
1	A Charge-Plasma-Based Transistor With Induced Graded Channel for Enhanced Analog Performance. IEEE Transactions on Electron Devices, 2016, 63, 2275-2281.	1.6	47
2	Improved performance of nanoscale junctionless transistor based on gate engineering approach. Microelectronics Reliability, 2015, 55, 318-325.	0.9	27
3	A Low Turn-Off Loss 4H-SiC Trench IGBT With Schottky Contact in the Collector Side. IEEE Transactions on Electron Devices, 2017, 64, 4575-4580.	1.6	13
4	3D Numerical Simulation of a Z Gate Layout MOSFET for Radiation Tolerance. Micromachines, 2018, 9, 659.	1.4	9
5	A Simulation Study of Sol-Like Bulk Silicon MOSFET With Improved Performance. IEEE Transactions on Electron Devices, 2014, 61, 3339-3344.	1.6	7
6	A Simulation Study of Hot Carrier Effects in Sol-Like Bulk Silicon nMOS Device. IEEE Transactions on Electron Devices, 2015, 62, 23-27.	1.6	5
7	Graded-channel junctionless dual-gate MOSFETs for radiation tolerance. Japanese Journal of Applied Physics, 2017, 56, 124201.	0.8	5
8	In-Built N+ Pocket Electrically Doped Tunnel FET With Improved DC and Analog/RF Performance. Micromachines, 2020, 11, 960.	1.4	5
9	A high-performance channel engineered charge-plasma-based MOSFET with high- $\hat{n}_e$ spacer. Superlattices and Microstructures, 2017, 112, 499-506.	1.4	4
10	Reliability improvements in SOI-like MOSFET with ESD and self-heating effect. Micro and Nano Letters, 2018, 13, 1649-1652.	0.6	4
11	Negative bias temperature instability in SOI-like p-type metal oxide semiconductor devices. Micro and Nano Letters, 2018, 13, 1151-1154.	0.6	0