Meng-Fan Chang

List of Publications by Year
in descending order

150 papers	5,427 citations	147566 31 h-index	149479 56 g-index
150 all docs	150 docs citations	150 times ranked	2979 citing authors

#	Article	IF	Citations
1	Two-Way Transpose Multibit 6T SRAM Computing-in-Memory Macro for Inference-Training AI Edge Chips. IEEE Journal of Solid-State Circuits, 2022, 57, 609-624.	3.5	18
2	A 40-nm, 64-Kb, 56.67 TOPS/W Voltage-Sensing Computing-In-Memory/Digital RRAM Macro Supporting Iterative Write With Verification and Online Read-Disturb Detection. IEEE Journal of Solid-State Circuits, 2022, 57, 68-79.	3.5	24
3	MARS: Multimacro Architecture SRAM CIM-Based Accelerator With Co-Designed Compressed Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1550-1562.	1.9	8
4	A 22-nm 1-Mb 1024-b Read Data-Protected STT-MRAM Macro With Near-Memory Shift-and-Rotate Functionality and 42.6-GB/s Read Bandwidth for Security-Aware Mobile Device. IEEE Journal of Solid-State Circuits, 2022, 57, 1936-1949.	3.5	7
5	A 40-nm 118.44-TOPS/W Voltage-Sensing Compute-in-Memory RRAM Macro With Write Verification and Multi-Bit Encoding. IEEE Journal of Solid-State Circuits, 2022, 57, 845-857.	3.5	22
6	STICKER-IM: A 65 nm Computing-in-Memory NN Processor Using Block-Wise Sparsity Optimization and Inter/Intra-Macro Data Reuse. IEEE Journal of Solid-State Circuits, 2022, 57, 2560-2573.	3.5	17
7	A 0.8V Intelligent Vision Sensor with Tiny Convolutional Neural Network and Programmable Weights Using Mixed-Mode Processing-in-Sensor Technique for Image Classification. , 2022, , .		10
8	Memristive technologies for data storage, computation, encryption, and radio-frequency communication. Science, 2022, 376, .	6.0	220
9	Concealable physically unclonable function chip with a memristor array. Science Advances, 2022, 8, .	4.7	27
10	In-memory Learning with Analog Resistive Switching Memory: A Review and Perspective. Proceedings of the IEEE, 2021, 109, 14-42.	16.4	96
11	A CMOS-integrated compute-in-memory macro based on resistive random-access memory for AI edge devices. Nature Electronics, 2021, 4, 81-90.	13.1	66
12	Challenges and Trends of SRAM-Based Computing-In-Memory for AI Edge Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1773-1786.	3.5	96
13	The role of government policy in the building of a global semiconductor industry. Nature Electronics, 2021, 4, 230-233.	13.1	5
14	Challenges of Computation-in-Memory Circuits for AI Edge Applications. , 2021, , .		2
15	A 40nm 1Mb 35.6 TOPS/W MLC NOR-Flash Based Computation-in-Memory Structure for Machine Learning. , 2021, , .		6
16	A Highly Reliable RRAM Physically Unclonable Function Utilizing Post-Process Randomness Source. IEEE Journal of Solid-State Circuits, 2021, 56, 1641-1650.	3.5	32
17	A 0.5-V Real-Time Computational CMOS Image Sensor With Programmable Kernel for Feature Extraction. IEEE Journal of Solid-State Circuits, 2021, 56, 1588-1596.	3.5	35
18	Efficient and Robust Nonvolatile Computing-In-Memory Based on Voltage Division in 2T2R RRAM With Input-Dependent Sensing Control. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1640-1644.	2.2	25

#	Article	IF	Citations
19	Sparsity-Aware Clamping Readout Scheme for High Parallelism and Low Power Nonvolatile Computing-in-Memory Based on Resistive Memory. , 2021, , .		2
20	STICKER-T: An Energy-Efficient Neural Network Processor Using Block-Circulant Algorithm and Unified Frequency-Domain Acceleration. IEEE Journal of Solid-State Circuits, 2021, 56, 1936-1948.	3.5	6
21	CiM3D: Comparator-in-Memory Designs Using Monolithic 3-D Technology for Accelerating Data-Intensive Applications. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 79-87.	1.1	2
22	A 0.8 V Multimode Vision Sensor for Motion and Saliency Detection With Ping-Pong PWM Pixel. IEEE Journal of Solid-State Circuits, 2021, 56, 2516-2524.	3.5	11
23	A Local Computing Cell and 6T SRAM-Based Computing-in-Memory Macro With 8-b MAC Operation for Edge AI Chips. IEEE Journal of Solid-State Circuits, 2021, 56, 2817-2831.	3.5	52
24	A 4T2R RRAM Bit Cell for Highly Parallel Ternary Content Addressable Memory. IEEE Transactions on Electron Devices, 2021, 68, 4933-4937.	1.6	15
25	Challenges and Trends of Nonvolatile In-Memory-Computation Circuits for AI Edge Devices. IEEE Open Journal of the Solid-State Circuits Society, 2021, 1, 171-183.	2.0	25
26	Challenge and Trend of SRAM Based Computation-in-Memory Circuits for AI Edge Devices. , 2021, , .		5
27	A four-megabit compute-in-memory macro with eight-bit precision based on CMOS and resistive random-access memory for AI edge devices. Nature Electronics, 2021, 4, 921-930.	13.1	36
28	Embedded 1-Mb ReRAM-Based Computing-in- Memory Macro With Multibit Input and Weight for CNN-Based AI Edge Processors. IEEE Journal of Solid-State Circuits, 2020, 55, 203-215.	3.5	62
29	A Twin-8T SRAM Computation-in-Memory Unit-Macro for Multibit CNN-Based AI Edge Processors. IEEE Journal of Solid-State Circuits, 2020, 55, 189-202.	3.5	108
30	A Two-way SRAM Array based Accelerator for Deep Neural Network On-chip Training. , 2020, , .		21
31	Neuro-inspired computing chips. Nature Electronics, 2020, 3, 371-382.	13.1	402
32	A 4-Kb 1-to-8-bit Configurable 6T SRAM-Based Computation-in-Memory Unit-Macro for CNN-Based AI Edge Processors. IEEE Journal of Solid-State Circuits, 2020, 55, 2790-2801.	3.5	50
33	A 28nm 1.5Mb Embedded 1T2R RRAM with 14.8 Mb/mm² using Sneaking Current Suppression and Compensation Techniques. , 2020, , .		13
34	15.2 A 28nm 64Kb Inference-Training Two-Way Transpose Multibit 6T SRAM Compute-in-Memory Macro for AI Edge Chips. , 2020, , .		99
35	15.5 A 28nm 64Kb 6T SRAM Computing-in-Memory Macro with 8b MAC Operation for AI Edge Chips. , 2020, , .		99
36	15.4 A 22nm 2Mb ReRAM Compute-in-Memory Macro with 121-28TOPS/W for Multibit MAC Computing for Tiny AI Edge Devices. , 2020, , .		97

#	Article	IF	Citations
37	14.3 A 65nm Computing-in-Memory-Based CNN Processor with 2.9-to-35.8TOPS/W System Energy Efficiency Using Dynamic-Sparsity Performance-Scaling Architecture and Energy-Efficient Inter/Intra-Macro Data Reuse. , 2020, , .		53
38	Challenges and Trends inDeveloping Nonvolatile Memory-Enabled Computing Chips for Intelligent Edge Devices. IEEE Transactions on Electron Devices, 2020, 67, 1444-1453.	1.6	35
39	Introduction to the Special Issue on the 2019 IEEE International Solid-State Circuits Conference (ISSCC). IEEE Journal of Solid-State Circuits, 2020, 55, 3-5.	3.5	0
40	33.2 A Fully Integrated Analog ReRAM Based 78.4TOPS/W Compute-In-Memory Chip with Fully Parallel MAC Computing. , 2020, , .		121
41	A 28-nm 320-Kb TCAM Macro Using Split-Controlled Single-Load 14T Cell and Triple-Margin Voltage Sense Amplifier. IEEE Journal of Solid-State Circuits, 2019, 54, 2743-2753.	3.5	21
42	Resistive Memoryâ€Based Inâ€Memory Computing: From Device and Largeâ€Scale Integration System Perspectives. Advanced Intelligent Systems, 2019, 1, 1900068.	3.3	54
43	A 5.1pJ/Neuron 127.3us/Inference RNN-based Speech Recognition Processor using 16 Computing-in-Memory SRAM Macros in 65nm CMOS. , 2019, , .		46
44	A 40nm 2Mb ReRAM Macro with 85% Reduction in FORMING Time and 99% Reduction in Page-Write Time Using Auto-FORMING and Auto-Write Schemes. , 2019, , .		13
45	Considerations of Integrating Computing-In-Memory and Processing-In-Sensor into Convolutional Neural Network Accelerators for Low-Power Edge Devices. , 2019, , .		5
46	Monolithic 3D+ -IC based Reconfigurable Compute-in-Memory SRAM Macro. , 2019, , .		8
47	A Dual-Split 6T SRAM-Based Computing-in-Memory Unit-Macro With Fully Parallel Product-Sum Operation for Binarized DNN Edge Processors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4172-4185.	3.5	93
48	RRAM-based Spiking Nonvolatile Computing-In-Memory Processing Engine with Precision-Configurable In Situ Nonlinear Activation. , 2019, , .		40
49	Threshold Switching Selectors: A Threshold Switching Selector Based on Highly Ordered Ag Nanodots for Xâ€Point Memory Applications (Adv. Sci. 10/2019). Advanced Science, 2019, 6, 1970058.	5.6	4
50	Monolithic-3D Integration Augmented Design Techniques for Computing in SRAMs. , 2019, , .		12
51	ROBIN: Monolithic-3D SRAM for Enhanced Robustness with In-Memory Computation Support. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2533-2545.	3.5	16
52	24.1 A 1Mb Multibit ReRAM Computing-In-Memory Macro with 14.6ns Parallel MAC Computing Time for CNN Based AI Edge Processors. , 2019, , .		162
53	24.5 A Twin-8T SRAM Computation-In-Memory Macro for Multiple-Bit CNN-Based Machine Learning. , 2019, , .		173
54	A Threshold Switching Selector Based on Highly Ordered Ag Nanodots for Xâ€Point Memory Applications. Advanced Science, 2019, 6, 1900024.	5.6	91

#	Article	IF	Citations
55	A 0.5V Real-Time Computational CMOS Image Sensor with Programmable Kernel for Always-On Feature Extraction. , 2019, , .		13
56	Challenges in Circuit Designs of Nonvolatile-memory based computing-in-memory for AI Edge Devices. , 2019, , .		3
57	AI Edge Devices Using Computing-In-Memory and Processing-In-Sensor: From System to Device. , 2019, , .		21
58	Monolithic 3D SRAM-CIM Macro Fabricated with BEOL Gate-All-Around MOSFETs. , 2019, , .		10
59	Circuit Design Challenges in Computing-in-Memory for AI Edge Devices. , 2019, , .		6
60	Recent Advances in Compute-in-Memory Support for SRAM Using Monolithic 3-D Integration. IEEE Micro, 2019, 39, 28-37.	1.8	3
61	A Few-Step and Low-Cost Memristor Logic Based on MIG Logic for Frequent-Off Instant-On Circuits in IoT Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 662-666.	2.2	12
62	A ReRAM Macro Using Dynamic Trip-Point-Mismatch Sampling Current-Mode Sense Amplifier and Low-DC Voltage-Mode Write-Termination Scheme Against Resistance and Write-Delay Variation. IEEE Journal of Solid-State Circuits, 2019, 54, 584-595.	3.5	14
63	A Threshold Switching Selector Based on Highly Ordered Ag Nanodots for X-Point Memory Applications. , 2019, 6, 1900024.		1
64	CMOS-integrated memristive non-volatile computing-in-memory for AI edge processors. Nature Electronics, 2019, 2, 420-428.	13.1	161
65	Compact 3-D-SRAM Memory With Concurrent Row and Column Data Access Capability Using Sequential Monolithic 3-D Integration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 671-683.	2.1	28
66	A Dual-Data Line Read Scheme for High-Speed Low-Energy Resistive Nonvolatile Memories. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 272-279.	2.1	5
67	Lowering Area Overheads for FeFET-Based Energy-Efficient Nonvolatile Flip-Flops. IEEE Transactions on Electron Devices, 2018, 65, 2670-2674.	1.6	21
68	A 65nm 1Mb nonvolatile computing-in-memory ReRAM macro with sub-16ns multiply-and-accumulate for binary DNN AI edge processors. , 2018, , .		169
69	A 65nm 4Kb algorithm-dependent computing-in-memory SRAM unit-macro with 2.3ns and 55.8TOPS/W fully parallel product-sum operation for binary DNN edge processors. , 2018, , .		106
70	Ultra-Low Power 3D NC-FinFET-based Monolithic 3D⁺ -IC with Computing-in-Memory for Intelligent IoT Devices. , 2018, , .		7
71	Sticker: A 0.41-62.1 TOPS/W 8Bit Neural Network Processor with Multi-Sparsity Compatible Convolution Arrays and Online Tuning Acceleration for Fully Connected Layers. , 2018, , .		86
72	DL-RSIM. , 2018, , .		50

#	Article	IF	Citations
73	Nonvolatile Circuits-Devices Interaction for Memory, Logic and Artificial Intelligence. , 2018, , .		22
74	A Full-Sensing-Margin Dual-Reference Sensing Scheme for Deeply-Scaled STT-RAM. IEEE Access, 2018, 6, 64250-64260.	2.6	6
75	Parallelizing SRAM arrays with customized bit-cell for binary neural networks. , 2018, , .		16
76	A Dual-Split-Controlled 4P2N 6T SRAM in Monolithic 3D-ICs With Enhanced Read Speed and Cell Stability for IoT Applications. IEEE Electron Device Letters, 2018, 39, 1167-1170.	2.2	5
77	A 1-V 2.6-mW Environmental Compensated Fully Integrated Nose-on-a-Chip. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1365-1369.	2.2	5
78	Guest Editorial Low-Power, Adaptive Neuromorphic Systems: Devices, Circuit, Architectures and Algorithms. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 1-5.	2.7	0
79	Data Backup Optimization for Nonvolatile SRAM in Energy Harvesting Sensor Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1660-1673.	1.9	20
80	Energy-Efficient TCAM Search Engine Design Using Priority-Decision in Memory Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 962-973.	2.1	14
81	A Flexible Wildcard-Pattern Matching Accelerator via Simultaneous Discrete Finite Automata. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3302-3316.	2.1	3
82	Design of Nonvolatile SRAM with Ferroelectric FETs for Energy-Efficient Backup and Restore. IEEE Transactions on Electron Devices, 2017, 64, 3037-3040.	1.6	48
83	A Compact-Area Low-VDDmin 6T SRAM With Improvement in Cell Stability, Read Speed, and Write Margin Using a Dual-Split-Control-Assist Scheme. IEEE Journal of Solid-State Circuits, 2017, 52, 2498-2514.	3.5	23
84	Advancing Nonvolatile Computing With Nonvolatile NCFET Latches and Flip-Flops. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2907-2919.	3.5	49
85	A 3T1R Nonvolatile TCAM Using MLC ReRAM for Frequent-Off Instant-On Filters in IoT and Big-Data Processing. IEEE Journal of Solid-State Circuits, 2017, 52, 1664-1679.	3.5	47
86	eTag: Tag-Comparison in Memory to Achieve Direct Data Access based on eDRAM to Improve Energy Efficiency of DRAM Cache. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 858-868.	3.5	8
87	A Resistance Drift Compensation Scheme to Reduce MLC PCM Raw BER by Over $100imes $ for Storage Class Memory Applications. IEEE Journal of Solid-State Circuits, 2017, 52, 218-228.	3.5	15
88	Improving FPGA Design with Monolithic 3D Integration Using High Dense Inter-Stack Via. , 2017, , .		6
89	Low-VDD Operation of SRAM Synaptic Array for Implementing Ternary Neural Network. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2962-2965.	2.1	19
90	A 65-nm ReRAM-Enabled Nonvolatile Processor With Time-Space Domain Adaption and Self-Write-Termination Achieving $> 4imes $ Faster Clock Frequency and $> 6imes $ Higher Restore Speed. IEEE Journal of Solid-State Circuits, 2017, 52, 2769-2785.	3.5	8

#	Article	IF	Citations
91	A ReRAM-Based Nonvolatile Flip-Flop With Self-Write-Termination Scheme for Frequent-OFF Fast-Wake-Up Nonvolatile Processors. IEEE Journal of Solid-State Circuits, 2017, 52, 2194-2207.	3.5	41
92	Enabling Energy-Efficient Nonvolatile Computing With Negative Capacitance FET. IEEE Transactions on Electron Devices, 2017, 64, 3452-3458.	1.6	72
93	TSV-free FinFET-based Monolithic 3D⁺-IC with computing-in-memory SRAM cell for intelligent IoT devices. , 2017, , .		24
94	A 16Mb dual-mode ReRAM macro with sub-14ns computing-in-memory and memory functions enabled by self-write termination scheme. , 2017, , .		36
95	A 462GOPs/J RRAM-based nonvolatile intelligent processor for energy harvesting IoE system featuring nonvolatile logics and processing-in-memory. , 2017, , .		3
96	Challenges of emerging memory and memristor based circuits: Nonvolatile logics, IoT security, deep learning and neuromorphic computing. , 2017, , .		9
97	a-SiGeC thin film photovoltaic enabled self-power monolithic 3D IC under indoor illumination. , 2016, , .		0
98	Design of a 0.5 V 1.68mW nose-on-a-chip for rapid screen of chronic obstructive pulmonary disease. , 2016, , .		2
99	A sub-0.5V charge pump circuit for resistive RAM (ReRAM) enabled low supply voltage nonvolatile logics and nonvoaltile processors. , 2016, , .		1
100	7.4 A 256b-wordlength ReRAM-based TCAM with 1ns search-time and 14Ã— improvement in wordlength-energyefficiency-density product using 2.5T1R cell. , 2016, , .		36
101	A Retention-Aware Multilevel Cell Phase Change Memory Program Evaluation Metric. IEEE Electron Device Letters, 2016, 37, 1422-1425.	2.2	5
102	Dilute manganese-doped ZnO nanowires for high photoelectrical performance. RSC Advances, 2016, 6, 91216-91224.	1.7	7
103	Designs of emerging memory based non-volatile TCAM for Internet-of-Things (IoT) and big-data processing: A 5T2R universal cell. , 2016, , .		23
104	A ReRAM-Based 4T2R Nonvolatile TCAM Using RC-Filtered Stress-Decoupled Scheme for Frequent-OFF Instant-ON Search Engines Used in IoT and Big-Data Processing. IEEE Journal of Solid-State Circuits, 2016, 51, 2786-2798.	3.5	26
105	4.7 A 65nm ReRAM-enabled nonvolatile processor with 6Ã— reduction in restore time and 4Ã— higher clock frequency using adaptive data retention and self-write-termination nonvolatile logic. , 2016, , .		53
106	Low-cost and TSV-free monolithic 3D-IC with heterogeneous integration of logic, memory and sensor analogy circuitry for Internet of Things. , 2015, , .		23
107	Challenges and Circuit Techniques for Energy-Efficient On-Chip Nonvolatile Memory Using Memristive Devices. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 183-193.	2.7	51
108	Logic/memory hybrid 3D sequentially integrated circuit using low thermal budget laser process. , 2015, , .		1

#	Article	IF	Citations
109	Set-Triggered-Parallel-Reset Memristor Logic for High-Density Heterogeneous-Integration Friendly Normally Off Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 80-84.	2.2	5
110	An Asymmetric-Voltage-Biased Current-Mode Sensing Scheme for Fast-Read Embedded Flash Macros. IEEE Journal of Solid-State Circuits, 2015, 50, 2188-2198.	3.5	17
111	Layer-Aware Program-and-Read Schemes for 3D Stackable Vertical-Gate BE-SONOS NAND Flash Against Cross-Layer Process Variations. IEEE Journal of Solid-State Circuits, 2015, 50, 1491-1501.	3.5	25
112	A New High-Density Twin-Gate Isolation One-Time Programmable Memory Cell in Pure 28-nm CMOS Logic Process. IEEE Transactions on Electron Devices, 2015, 62, 121-127.	1.6	9
113	Energy-efficient non-volatile TCAM search engine design using priority-decision in memory technology for DPI. , 2015, , .		12
114	Low <formula formulatype="inline"><tex Notation="TeX">${m VDDmin}$</tex></formula> Swing-Sample-and-Couple Sense Amplifier and Energy-Efficient Self-Boost-Write-Termination Scheme for Embedded ReRAM Macros Against Resistance and Switch-Time Variations. IEEE Journal of Solid-State Circuits, 2015, 50, 2786-2795.	3.5	25
115	An Energy Efficient Backup Scheme with Low Inrush Current for Nonvolatile SRAM in Energy Harvesting Sensor Nodes. , 2015, , .		19
116	A Fully Integrated Nose-on-a-Chip for Rapid Diagnosis of Ventilator-Associated Pneumonia. IEEE Transactions on Biomedical Circuits and Systems, 2014, 8, 765-778.	2.7	22
117	A signal acquisition and processing chip with built-in cluster for chemiresistive gas sensor array. , 2014, , .		1
118	19.4 embedded 1Mb ReRAM in 28nm CMOS with 0.27-to-1V read using swing-sample-and-couple sense amplifier and self-boost-write-termination scheme. , 2014, , .		76
119	Area-Efficient Embedded Resistive RAM (ReRAM) Macros Using Logic-Process Vertical-Parasitic-BJT (VPBJT) Switches and Read-Disturb-Free Temperature-Aware Current-Mode Read Scheme. IEEE Journal of Solid-State Circuits, 2014, 49, 908-916.	3.5	20
120	A Sub-0.3 V Area-Efficient L-Shaped 7T SRAM With Read Bitline Swing Expansion Schemes Based on Boosted Read-Bitline, Asymmetric-V$_{m TH}$ Read-Port, and Offset Cell VDD Biasing Techniques. IEEE Journal of Solid-State Circuits, 2013, 48, 2558-2569.	3.5	46
121	A Low-Voltage Bulk-Drain-Driven Read Scheme for Sub-0.5 V 4 Mb 65 nm Logic-Process Compatible Embedded Resistive RAM (ReRAM) Macro. IEEE Journal of Solid-State Circuits, 2013, 48, 2250-2259.	3.5	24
122	A High Layer Scalability TSV-Based 3D-SRAM With Semi-Master-Slave Structure and Self-Timed Differential-TSV for High-Performance Universal-Memory-Capacity-Platforms. IEEE Journal of Solid-State Circuits, 2013, 48, 1521-1529.	3.5	13
123	Low-Voltage Embedded NAND-ROM Macros Using Data-Aware Sensing Reference Scheme for VDDmin, Speed and Power Improvement. IEEE Journal of Solid-State Circuits, 2013, 48, 611-623.	3.5	10
124	Monolithic 3D chip integrated with 500ns NVM, 3ps logic circuits and SRAM. , 2013, , .		32
125	An Offset-Tolerant Fast-Random-Read Current-Sampling-Based Sense Amplifier for Small-Cell-Current Nonvolatile Memory. IEEE Journal of Solid-State Circuits, 2013, 48, 864-877.	3.5	83
126	A High-Speed 7.2-ns Read-Write Random Access 4-Mb Embedded Resistive RAM (ReRAM) Macro Using Process-Variation-Tolerant Current-Mode Read Schemes. IEEE Journal of Solid-State Circuits, 2013, 48, 878-891.	3.5	81

#	Article	IF	Citations
127	Strengthening Modern Electronics Industry Through the National Program for Intelligent Electronics in Taiwan. IEEE Access, 2013, 1, 123-130.	2.6	3
128	A ReRAM integrated 7T2R non-volatile SRAM for normally-off computing application. , 2013, , .		40
129	Circuit design challenges and trends in read sensing schemes for resistive-type emerging nonvolatile memory. , 2012, , .		5
130	Low Store Energy, Low VDDmin, 8T2R Nonvolatile Latch and SRAM With Vertical-Stacked Resistive Memory (Memristor) Devices for Low Power Mobile Applications. IEEE Journal of Solid-State Circuits, 2012, 47, 1483-1496.	3.5	132
131	Endurance-aware circuit designs of nonvolatile logic and nonvolatile sram using resistive memory (memristor) device. , 2012, , .		31
132	A 45-nm Dual-Port SRAM Utilizing Write-Assist Cells Against Simultaneous Access Disturbances. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 790-794.	2.2	16
133	Compact Measurement Schemes for Bit-Line Swing, Sense Amplifier Offset Voltage, and Word-Line Pulse Width to Characterize Sensing Tolerance Margin in a 40 nm Fully Functional Embedded SRAM. IEEE Journal of Solid-State Circuits, 2012, 47, 969-980.	3.5	11
134	Circuit design challenges in embedded memory and resistive RAM (RRAM) for mobile SoC and 3D-IC. , 2011, , .		17
135	A 130 mV SRAM With Expanded Write and Read Margins for Subthreshold Applications. IEEE Journal of Solid-State Circuits, 2011, 46, 520-529.	3.5	111
136	A Large $sigma V_{m TH}$/VDD Tolerant Zigzag 8T SRAM With Area-Efficient Decoupled Differential Sensing and Fast Write-Back Scheme. IEEE Journal of Solid-State Circuits, 2011, 46, 815-827.	3.5	65
137	A Low-Power Electronic Nose Signal-Processing Chip for a Portable Artificial Olfaction System. IEEE Transactions on Biomedical Circuits and Systems, 2011, 5, 380-390.	2.7	56
138	Three-Dimensional $hbox{4F}^{2}$ ReRAM With Vertical BJT Driver by CMOS Logic Compatible Process. IEEE Transactions on Electron Devices, 2011, 58, 2466-2472.	1.6	26
139	A wearable Electronic Nose SoC for healthier living. , 2011, , .		7
140	Embedded non-volatile memory circuit design technologies for mobile low-voltage SoC and 3D-IC. , 2010, , .		4
141	A 0.45-V 300-MHz 10T Flowthrough SRAM With Expanded write/ read Stability and Speed-Area-Wise Array for Sub-0.5-V Chips. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 980-985.	2.2	14
142	A Differential Data-Aware Power-Supplied (D^{2}AP) 8T SRAM Cell With Expanded Write/Read Stabilities for Lower VDDmin Applications. IEEE Journal of Solid-State Circuits, 2010, 45, 1234-1245.	3.5	54
143	Noise-Immune Embedded NAND-ROM Using a Dynamic Split Source-Line Scheme for VDDmin and Speed Improvements. IEEE Journal of Solid-State Circuits, 2010, 45, 2142-2155.	3.5	6
144	Analysis and Reduction of Supply Noise Fluctuations Induced by Embedded Via-Programming ROM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 758-769.	2.1	13

#	Article	IF	Citations
145	A Wide-VDD Embedded SRAM for Dynamic Voltage Asynchronous Systems. , 2009, , .		0
146	Wide $V_{m DD}$ Embedded Asynchronous SRAM With Dual-Mode Self-Timed Technique for Dynamic Voltage Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1657-1667.	3.5	30
147	A Process Variation Tolerant Embedded Split-Gate Flash Memory Using Pre-Stable Current Sensing Scheme. IEEE Journal of Solid-State Circuits, 2009, 44, 987-994.	3.5	37
148	Experiments on reducing standby current for compilable SRAM using hidden clustered source line control. , 2007, , .		1
149	Improving the speed and power of compilable SRAM using dual-mode self-timed technique. Memory Technology, Design and Testing (MTDT), IEEE International Workshop on, 2007, , .	0.0	3
150	A Full Code-Patterns Coverage High-Speed Embedded ROM Using Dynamic Virtual Guardian Technique. IEEE Journal of Solid-State Circuits, 2006, 41, 496-506.	3.5	14