Jingtong Hu

List of Publications by Year
in descending order

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143 papers	2,522 citations	393982 19 h-index	360668 35 g-index
143 all docs	143 docs citations	143 times ranked	1433 citing authors

#	Article	IF	Citations
1	Toward Comprehensive Shifting Fault Tolerance for Domain-Wall Memories With PIETT. IEEE Transactions on Computers, 2023, 72, 1095-1109.	2.4	5
2	Cooperative Communication Between Two Transiently Powered Sensor Nodes by Reinforcement Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 76-90.	1.9	9
3	Personalized Neural Network for Patient-Specific Health Monitoring in IoT: A Metalearning Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 5394-5407.	1.9	5
4	Energy-Aware Adaptive Multi-Exit Neural Network Inference Implementation for a Millimeter-Scale Sensing System. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 849-859.	2.1	5
5	Device-Circuit-Architecture Co-Exploration for Computing-in-Memory Neural Accelerators. IEEE Transactions on Computers, 2021, 70, 595-605.	2.4	37
6	DAC-SDC Low Power Object Detection Challenge for UAV Applications. IEEE Transactions on Pattern Analysis and Machine Intelligence, 2021, 43, 392-403.	9.7	43
7	Lightweight Run-Time Working Memory Compression for Deployment of Deep Neural Networks on Resource-Constrained MCUs. , 2021, , .		8
8	Developing a Miniature Energy-Harvesting-Powered Edge Device with Multi-Exit Neural Network. , 2021, , .		5
9	Learning to Learn Personalized Neural Network for Ventricular Arrhythmias Detection on Intracardiac EGMs. , 2021, , .		6
10	Implementation of Multi-Exit Neural-Network Inferences for an Image-Based Sensing System with Energy Harvesting. Journal of Low Power Electronics and Applications, 2021, 11, 34.	1.3	5
11	Algorithm-hardware Co-design of Attention Mechanism on FPGA Devices. Transactions on Embedded Computing Systems, 2021, 20, 1-24.	2.1	14
12	Federated Contrastive Learning for Dermatological Disease Diagnosis via On-device Learning (Invited) Tj ETQq0 0 0 rgBT /Overlock 10 Tf		9
13	Enabling On-Device CNN Training by Self-Supervised Instance Filtering and Error Map Pruning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3445-3457.	1.9	20
14	Standing on the Shoulders of Giants: Hardware and Neural Architecture Co-Search With Hot Start. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4154-4165.	1.9	40
15	Communication-Aware Task Scheduling for Energy-Harvesting Nonvolatile Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1796-1806.	2.1	7
16	Hardware/Software Co-Exploration of Neural Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4805-4815.	1.9	86
17	Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence. , 2020, , .		22
18	Intermittent Inference with Nonuniformly Compressed Multi-Exit Neural Network for Energy Harvesting Powered Devices. , 2020, , .		18

#	Article	IF	Citations
19	Achieving Full Parallelism in LSTM via a Unified Accelerator Design. , 2020, , .		6
20	Low Overhead Online Data Flow Tracking for Intermittently Powered Non-Volatile FPGAs. ACM Journal on Emerging Technologies in Computing Systems, 2020, 16, 1-20.	1.8	5
21	Applying Multiple Level Cell to Non-volatile FPGAs. Transactions on Embedded Computing Systems, 2020, 19, 1-22.	2.1	5
22	Towards cardiac intervention assistance. , 2020, , .		4
23	On the Design of Time-Constrained and Buffer-Optimal Self-Timed Pipelines. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1515-1528.	1.9	1
24	Real-Time Data Retrieval in Cyber-Physical Systems with Temporal Validity and Data Availability Constraints. IEEE Transactions on Knowledge and Data Engineering, 2019, 31, 1779-1793.	4.0	6
25	Guest Editorial: IEEE Transactions on Computers Special Section on Emerging Non-Volatile Memory Technologies: From Devices to Architectures and Systems. IEEE Transactions on Computers, 2019, 68, 1111-1113.	2.4	4
26	Accuracy vs. Efficiency. , 2019, , .		92
27	Achieving Super-Linear Speedup across Multi-FPGA for Real-Time DNN Inference. Transactions on Embedded Computing Systems, 2019, 18, 1-23.	2.1	49
28	When Neural Architecture Search Meets Hardware Implementation: from Hardware Awareness to Co-Design. , 2019, , .		18
29	In-memory AES Implementation for Emerging Non-Volatile Main Memory. , 2019, , .		1
30	Modeling and Optimization for Self-powered Non-volatile IoT Edge Devices with Ultra-low Harvesting Power. ACM Transactions on Cyber-Physical Systems, 2019, 3, 1-26.	1.9	12
31	Cooperative communication between two transiently powered sensors by reinforcement learning. , 2019, , .		1
32	Checkpointing-Aware Loop Tiling for Energy Harvesting Powered Nonvolatile Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 15-28.	1.9	11
33	XFER. , 2019, , .		10
34	AIM: Fast and energy-efficient AES in-memory implementation for emerging non-volatile main memory. , 2018, , .		11
35	Avoiding Data Inconsistency in Energy Harvesting Powered Embedded Systems. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-25.	1.9	17
36	Prototyping Energy Harvesting Powered Systems with Nonvolatile Processor (Invited Paper). , 2018, , .		2

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37	Write Energy Reduction for PCM via Pumping Efficiency Improvement. ACM Transactions on Storage, 2018, 14, 1-21.	1.4	1
38	ENZYME: An Energy-Efficient Transient Computing Paradigm for Ultralow Self-Powered IoT Edge Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2440-2450.	1.9	20
39	Securing Emerging Nonvolatile Main Memory With Fast and Energy-Efficient AES In-Memory Implementation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2443-2455.	2.1	13
40	Heterogeneous FPGA-Based Cost-Optimal Design for Timing-Constrained CNNs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2542-2554.	1.9	28
41	NVM-Based FPGA Block RAM With Adaptive SLC-MLC Conversion. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2661-2672.	1.9	9
42	State Asymmetry Driven State Remapping in Phase Change Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 27-40.	1.9	12
43	Stack-Size Sensitive On-Chip Memory Backup for Self-Powered Nonvolatile Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1804-1816.	1.9	24
44	Exploiting Multiple Write Modes of Nonvolatile Main Memory in Embedded Systems. Transactions on Embedded Computing Systems, 2017, 16, 1-26.	2.1	11
45	Multisource Indoor Energy Harvesting for Nonvolatile Processors. IEEE Design and Test, 2017, 34, 42-49.	1.1	9
46	CP-FPGA: Energy-Efficient Nonvolatile FPGA With Offline/Online Checkpointing Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2153-2163.	2.1	5
47	A lightweight progress maximization scheduler for non-volatile processor under unstable energy harvesting. , 2017, , .		9
48	Age-aware Logic and Memory Co-Placement for RRAM-FPGAs. , 2017, , .		13
49	vFlash: Virtualized Flash for Optimizing the I/O Performance in Mobile Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1203-1214.	1.9	11
50	FlexLevel NAND Flash Storage System Design to Reduce LDPC Latency. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1167-1180.	1.9	14
51	CNN-based pattern recognition on nonvolatile IoT platform for smart ultraviolet monitoring: (Invited) Tj ETQq1 1 0.784314 rgBT /Ove		1
52	Maximize energy utilization for ultra-low energy harvesting powered embedded systems. , 2017, , .		3
53	Design Exploration for Multiple Level Cell Based Non-Volatile FPGAs. , 2017, , .		4
54	Runtime and reconfiguration dual-aware placement for SRAM-NVM hybrid FPGAs. , 2017, , .		3

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55	A lightweight progress maximization scheduler for non-volatile processor under unstable energy harvesting. ACM SIGPLAN Notices, 2017, 52, 101-110.	0.2	11
56	An Efficient Racetrack Memory-Based Processing-in-Memory Architecture for Convolutional Neural Networks. , 2017, , .		10
57	Redesigning software and systems for non-volatile processors on self-powered devices. , 2016, , .		13
58	A Time, Energy, and Area Efficient Domain Wall Memory-Based SPM for Embedded Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 2008-2017.	1.9	17
59	Peak-to-average pumping efficiency improvement for charge pump in Phase Change Memories. , 2016, , .		3
60	Multi-source in-door energy harvesting for non-volatile processors. , 2016, , .		8
61	Two-step state transition minimization for lifetime and performance improvement on MLC STT-RAM. , 2016, , .		20
62	TEMP. , 2016, , .		8
63	Neural Network-based Prediction Algorithms for In-Door Multi-Source Energy Harvesting System for Non-Volatile Processors. , 2016, , .		5
64	Dynamic converter reconfiguration for near-threshold non-volatile processors using in-door energy harvesting. , 2016, , .		1
65	Ring-shaped Racetrack memory based on spin orbit torque driven chiral domain wall motions. Scientific Reports, 2016, 6, 35062.	1.6	17
66	Checkpoint aware hybrid cache architecture for NV processor in energy harvesting powered systems. , 2016, , .		28
67	Image-Content-Aware I/O Optimization for Mobile Virtualization. Transactions on Embedded Computing Systems, 2016, 16, 1-24.	2.1	7
68	Performance-aware task scheduling for energy harvesting nonvolatile processors considering power switching overhead. , 2016, , .		7
69	Routing path reuse maximization for efficient NV-FPGA reconfiguration. , 2016, , .		12
70	Wear-Leveling Aware Page Management for Non-Volatile Main Memory on Embedded Systems. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 129-142.	2.5	16
71	Write Mode Aware Loop Tiling for High Performance Low Power Volatile PCM in Embedded Systems. IEEE Transactions on Computers, 2016, 65, 2313-2324.	2.4	6
72	Data Allocation with Minimum Cost under Guaranteed Probability for Multiple Types of Memories. Journal of Signal Processing Systems, 2016, 84, 151-162.	1.4	5

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73	Multi-source energy harvesting management and optimization for non-volatile processors. , 2015, , .		8
74	Nonvolatile main memory aware garbage collection in high-level language virtual machine. , 2015, , .		3
75	Virtual Machine Image Content Aware I/O Optimization for Mobile Virtualization. , 2015, , .		3
76	Non-volatile memories in FPGAs: Exploiting logic similarity to accelerate reconfiguration and increase programming cycles. , 2015, , .		4
77	Reliability-Guaranteed Task Assignment and Scheduling for Heterogeneous Multiprocessors Considering Timing Constraint. Journal of Signal Processing Systems, 2015, 81, 359-375.	1.4	14
78	Unified non-volatile memory and NAND flash memory architecture in smartphones. , 2015, , .		17
79	Checkpoint-aware instruction scheduling for nonvolatile processor with multiple functional units. , 2015, , .		5
80	Improving performance and lifetime of DRAM-PCM hybrid main memory through a proactive page allocation strategy. , 2015, , .		24
81	Area and performance co-optimization for domain wall memory in application-specific embedded systems. , 2015, , .		19
82	Compiler directed automatic stack trimming for efficient non-volatile processors. , 2015, , .		25
83	FlexLevel. , 2015, , .		18
84	VWS. , 2015, , .		5
85	Fine-tuning CLB placement to speed up reconfigurations in NVM-based FPGAs. , 2015, , .		14
86	Fixing the broken time machine. , 2015, , .		64
87	Optimizing Task and Data Assignment on Multi-Core Systems with Multi-Port SPMs. IEEE Transactions on Parallel and Distributed Systems, 2015, 26, 2549-2560.	4.0	14
88	Low Overhead Software Wear Leveling for Hybrid PCM + DRAM Main Memory on Embedded Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 654-663.	2.1	28
89	Software Assisted Non-volatile Register Reduction for Energy Harvesting Based Cyber-Physical System. , 2015, , .		19
90	Stream Bench: Towards Benchmarking Modern Distributed Stream Computing Frameworks. , 2014, , .		65

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91	3M-PCM. , 2014, , .		20
92	Online Data Allocation for Hybrid Memories on Embedded Tele-health Systems. , 2014, , .		29
93	Wear-leveling for PCM main memory on embedded system via page management and process scheduling. , 2014, , .		4
94	Management and optimization for nonvolatile memory-based hybrid scratchpad memory on multicore embedded processors. Transactions on Embedded Computing Systems, 2014, 13, 1-25.	2.1	21
95	Virtual-machine metadata optimization for I/O traffic reduction in mobile virtualization. , 2014, , .		3
96	Scheduling to Optimize Cache Utilization for Non-Volatile Main Memories. IEEE Transactions on Computers, 2014, 63, 2039-2051.	2.4	7
97	Non-volatile registers aware instruction selection for embedded systems. , 2014, , .		3
98	A space allocation and reuse strategy for PCM-based embedded systems. Journal of Systems Architecture, 2014, 60, 655-667.	2.5	8
99	Minimizing System Cost with Efficient Task Assignment on Heterogeneous Multicore Processors Considering Time Constraint. IEEE Transactions on Parallel and Distributed Systems, 2014, 25, 2101-2113.	4.0	28
100	Minimum-cost data allocation with guaranteed probability on multiple types of memory. , 2014, , .		0
101	A genetic algorithm for task scheduling on heterogeneous computing systems using multiple priority queues. Information Sciences, 2014, 270, 255-287.	4.0	317
102	Efficient grouping-based mapping and scheduling on heterogeneous cluster architectures. Computers and Electrical Engineering, 2014, 40, 1604-1620.	3.0	5
103	Efficient Loop Scheduling for Chip Multiprocessors with Non-Volatile Main Memory. Journal of Signal Processing Systems, 2013, 71, 261-273.	1.4	5
104	Algorithms to Minimize Data Transfer for Code Update on Wireless Sensor Network. Journal of Signal Processing Systems, 2013, 71, 143-157.	1.4	0
105	Energy-aware preemptive scheduling algorithm for sporadic tasks on DVS platform. Microprocessors and Microsystems, 2013, 37, 99-112.	1.8	40
106	Data Allocation Optimization for Hybrid Scratch Pad Memory With SRAM and Nonvolatile Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1094-1102.	2.1	54
107	Data Placement and Duplication for Embedded Multicore Systems With Scratch Pad Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 809-817.	1.9	52
108	Minimizing accumulative memory load cost on multi-core DSPs with multi-level memory. Journal of Systems Architecture, 2013, 59, 389-399.	2.5	5

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109	Optimal data allocation algorithm for loop-centric applications on scratch-PAD memories. , 2013, , .		0
110	A space-based wear leveling for PCM-based embedded systems. , 2013, , .		7
111	Optimizing task assignment for heterogeneous multiprocessor system with guaranteed reliability and timing constraint. , 2013, , .		0
112	Write activity reduction on non-volatile main memories for embedded chip multiprocessors. Transactions on Embedded Computing Systems, 2013, 12, 1-27.	2.1	42
113	Software Enabled Wear-Leveling for Hybrid PCM Main Memory on Embedded Systems. , 2013, , .		46
114	Efficient task assignment and scheduling for MPSoC DSPS with VS-SPM considering concurrent accesses through data allocation. , 2013, , .		3
115	MGC: Multiple graph-coloring for non-volatile memory based hybrid Scratchpad Memory. , 2012, , .		13
116	Loop scheduling optimization for chip-multiprocessors with non-volatile main memory. , 2012, , .		8
117	Randomized execution algorithms for smart cards to resist power analysis attacks. Journal of Systems Architecture, 2012, 58, 426-438.	2.5	1
118	PRR: A low-overhead cache replacement algorithm for embedded processors. , 2012, , .		0
119	Optimizing Data Allocation and Memory Configuration for Non-Volatile Memory Based Hybrid SPM on Embedded CMPs. , 2012, , .		10
120	Minimizing Access Cost for Multiple Types of Memory Units in Embedded Systems Through Data Allocation and Scheduling. IEEE Transactions on Signal Processing, 2012, 60, 3253-3263.	3.2	25
121	CAR: Securing PCM Main Memory System with Cache Address Remapping. , 2012, , .		24
122	Optimal Assignment for Tree-Structure Task Graph on Heterogeneous Multicore Systems Considering Time Constraint. , 2012, , .		5
123	Memory access schedule minimization for embedded systems. Journal of Systems Architecture, 2012, 58, 48-59.	2.5	5
124	Efficient Task Assignment on Heterogeneous Multicore Systems Considering Communication Overhead. Lecture Notes in Computer Science, 2012, , 171-185.	1.0	2
125	Towards energy efficient hybrid on-chip Scratch Pad Memory with non-volatile memory. , 2011, , .		28
126	Optimal Data Allocation for Scratch-Pad Memory on Embedded Multi-core Systems. , 2011, , .		89

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127	Optimal Data Placement for Memory Architectures with Scratch-Pad Memories. , 2011, , .		3
128	Write Activity Minimization for Nonvolatile Main Memory Via Scheduling and Recomputation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 584-592.	1.9	42
129	Algorithms for Optimally Arranging Multicore Memory Structures. Eurasip Journal on Embedded Systems, 2010, 2010, 871510.	1.2	0
130	Write activity reduction on flash main memory via smart victim cache. , 2010, , .		48
131	Reducing write activities on non-volatile memories in embedded CMPs via data migration and recomputation. , 2010, , .		96
132	Iterational retiming with partitioning. Transactions on Embedded Computing Systems, 2010, 9, 1-26.	2.1	16
133	Impacts of Inaccurate Information on Resource Allocation for Multi-Core Embedded Systems. , 2010, , .		3
134	Minimizing write activities to non-volatile memory via scheduling and recomputation. , 2010, , .		15
135	Optimal scheduling to minimize non-volatile memory access time with hardware cache. , 2010, , .		5
136	Thermal-aware rotation scheduling for 3D multi-core with timing constraint. , 2010, , .		6
137	Optimizing Scheduling and Intercluster Connection for Application-Specific DSP Processors. IEEE Transactions on Signal Processing, 2009, 57, 4538-4547.	3.2	6
138	Minimizing Memory Access Schedule for Memories. , 2009, , .		2
139	Energy Minimization and Latency Hiding for Heterogeneous Parallel Memory. , 2009, , .		0
140	Reprogramming with Minimal Transferred Data on Wireless Sensor Network. , 2009, , .		21
141	Timing optimization via nest-loop pipelining considering code size. Microprocessors and Microsystems, 2008, 32, 351-363.	1.8	9
142	Address assignment sensitive variable partitioning and scheduling for DSPS with multiple memory banks. Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing, 2008, , .	1.8	9
143	Dynamic and Leakage Power Minimization with Loop Voltage Scheduling and Assignment. , 2008, , .		0