Juha Plosila

List of Publications by Year
in descending order

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241	3,816	430843	265191
papers	citations	18	42
		h-index	g-index

242	242	242	2428
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	DBA-Filter: A Dynamic Background Activity Noise Filtering Algorithm forÂEvent Cameras. Lecture Notes in Networks and Systems, 2022, , 685-696.	0.7	4
2	Cellular Formation Maintenance andÂCollision Avoidance Using Centroid-Based Point Set Registration inÂaÂSwarm of Drones. Lecture Notes in Networks and Systems, 2022, , 391-408.	0.7	2
3	Real-Time Classification of Pain Level Using Zygomaticus and Corrugator EMG Features. Electronics (Switzerland), 2022, 11, 1671.	3.1	3
4	Low-cost ultrasonic based object detection and collision avoidance method for autonomous robots. International Journal of Information Technology (Singapore), 2021, 13, 97-107.	2.7	17
5	Dynamic Resource-Aware Corner Detection for Bio-Inspired Vision Sensors. , 2021, , .		5
6	SB-Router: A Swapped Buffer Activated Low Latency Network-on-Chip Router. IEEE Access, 2021, 9, 126564-126578.	4.2	7
7	Dynamic Formation Reshaping Based on Point Set Registration in a Swarm of Drones. Advances in Intelligent Systems and Computing, 2021, , 577-588.	0.6	2
8	Energy-Efficient Navigation of an Autonomous Swarm with Adaptive Consciousness. Remote Sensing, 2021, 13, 1059.	4.0	10
9	Swarm formation morphing for congestion-aware collision avoidance. Heliyon, 2021, 7, e07840.	3.2	9
10	A Resource Management Model for Distributed Multi-Task Applications in Fog Computing Networks. IEEE Access, 2021, 9, 152792-152802.	4.2	3
11	Energy-Efficient Mobile Robot Control via Run-time Monitoring of Environmental Complexity and Computing Workload. , 2021, , .		0
12	Particle telescope aboard FORESAIL-1: Simulated performance. Advances in Space Research, 2020, 66, 29-41.	2.6	3
13	GeFeS: A generalized wrapper feature selection approach for optimizing classification performance. Computers in Biology and Medicine, 2020, 125, 103974.	7.0	40
14	Energy-Efficient Formation Morphing for Collision Avoidance in a Swarm of Drones. IEEE Access, 2020, 8, 170681-170695.	4.2	25
15	Comparison of Linear and Nonlinear Methods for Distributed Control of a Hierarchical Formation of UAVs. IEEE Access, 2020, 8, 95667-95680.	4.2	17
16	Unmanned Aerial Vehicles (UAVs): Collision Avoidance Systems and Approaches. IEEE Access, 2020, 8, 105139-105155.	4.2	158
17	Heterogeneous Parallelization for Object Detection and Tracking in UAVs. IEEE Access, 2020, 8, 42784-42793.	4.2	13
18	Navigation of Autonomous Swarm of Drones Using Translational Coordinates. Lecture Notes in Computer Science, 2020, , 353-362.	1.3	8

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19	Night vision obstacle detection and avoidance based on Bio-Inspired Vision Sensors. , 2020, , .		5
20	Implementation of non-intrusive appliances load monitoring (NIALM) on k-nearest neighbors (k-NN) classifier. AIMS Electronics and Electrical Engineering, 2020, 4, 326-344.	1.5	9
21	Asynchronous Corner Tracking Algorithm Based on Lifetime of Events for DAVIS Cameras. Lecture Notes in Computer Science, 2020, , 530-541.	1.3	3
22	A Survey on Odometry for Autonomous Navigation Systems. IEEE Access, 2019, 7, 97466-97486.	4.2	115
23	Swarms of Unmanned Aerial Vehicles â€" A Survey. Journal of Industrial Information Integration, 2019, 16, 100106.	6.4	147
24	Formation Maintenance and Collision Avoidance in a Swarm of Drones. , 2019, , .		16
25	Parallel imperialist competitive algorithms. Concurrency Computation Practice and Experience, 2018, 30, e4393.	2.2	7
26	Hierarchal Placement of Smart Mobile Access Points in Wireless Sensor Networks Using Fog Computing. , 2017, , .		8
27	Placement of Smart Mobile Access Points in Wireless Sensor Networks and Cyber-Physical Systems Using Fog Computing. , 2016, , .		9
28	An Approach for Smart Management of Big Data in the Fog Computing Context. , 2016, , .		16
29	PICA: Multi-population Implementation of Parallel Imperialist Competitive Algorithms. , 2016, , .		9
30	Multi-population parallel imperialist competitive algorithm for solving systems of nonlinear equations. , 2016, , .		4
31	SEECC: A secure and efficient elliptic curve cryptosystem for E-health applications. , 2016, , .		1
32	A Power-Aware Approach for Online Test Scheduling in Many-Core Architectures. IEEE Transactions on Computers, 2016, 65, 730-743.	3.4	12
33	Polymorphic Configuration Architecture for CGRAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 403-407.	3.1	4
34	PDNOC: Partially diagonal networkâ€onâ€chip for high efficiency multicore systems. Concurrency Computation Practice and Experience, 2015, 27, 1054-1067.	2.2	7
35	Architecture and Implementation of Dynamic Parallelism, Voltage and Frequency Scaling (PVFS) on CGRAs. ACM Journal on Emerging Technologies in Computing Systems, 2015, 11, 1-29.	2.3	3
36	Trio: A Triple Class On-chip Network Design for Efficient Multicore Processors. , 2015, , .		2

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37	A Low-Overhead, Fully-Distributed, Guaranteed-Delivery Routing Algorithm for Faulty Network-on-Chips. , 2015, , .		17
38	Using Ant Colony System to Consolidate VMs for Green Cloud Computing. IEEE Transactions on Services Computing, 2015, 8, 187-198.	4.6	256
39	DyMeP: An Infrastructure to Support Dynamic Memory Binding for Runtime Mapping in CGRAs. , 2015, , .		4
40	TEA: Timing and Energy Aware compression architecture for Efficient Configuration in CGRAs. Microprocessors and Microsystems, 2015, 39, 973-986.	2.8	1
41	FIST: A Framework to Interleave Spiking Neural Networks on CGRAs. , 2015, , .		3
42	Dynamic power management for many-core platforms in the dark silicon era: A multi-objective control approach. , 2015, , .		33
43	Utilization Prediction Aware VM Consolidation Approach for Green Cloud Computing. , 2015, , .		58
44	Parallel Implementation of Fuzzified Pattern Matching Algorithm on GPU. , 2015, , .		3
45	In-order delivery approach for 2D and 3D NoCs. Journal of Supercomputing, 2015, 71, 2877-2899.	3.6	2
46	High Performance Pattern Matching on Heterogeneous Platform. Journal of Integrative Bioinformatics, 2014, 11, 88-98.	1.5	2
47	Energy-efficient concurrent testing approach for many-core systems in the dark silicon age. , 2014, , .		2
48	Dark silicon aware power management for manycore systems under dynamic workloads. , 2014, , .		29
49	Hierarchical Agent-Based Architecture for Resource Management in Cloud Data Centers. , 2014, , .		4
50	Multi-agent Based Architecture for Dynamic VM Consolidation in Cloud Data Centers. , 2014, , .		15
51	Energy-Aware Dynamic VM Consolidation in Cloud Data Centers Using Ant Colony System. , 2014, , .		32
52	Morphable Compression Architecture for Efficient Configuration in CGRAs. , 2014, , .		3
53	SHiFA. , 2014, , .		9
54	Timepix3: a 65K channel hybrid pixel readout chip with simultaneous ToA/ToT and sparse readout. Journal of Instrumentation, 2014, 9, C05013-C05013.	1.2	351

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55	Hierarchical VM Management Architecture for Cloud Data Centers. , 2014, , .		15
56	From self-aware building blocks to self-organizing systems with hierarchical agent-based adaptation. , 2014, , .		1
57	TransPar: Transformation based dynamic Parallelism for low power CGRAs. , 2014, , .		3
58	Parameterized AES-Based Crypto Processor for FPGAs. , 2014, , .		8
59	Online testing of many-core systems in the Dark Silicon era. , 2014, , .		4
60	Silicon synapse designs for VLSI neuromorphic platform. , 2014, , .		1
61	Private reliability environments for efficient fault-tolerance in CGRAs. Design Automation for Embedded Systems, 2014, 18, 295-327.	1.0	2
62	Energy-Efficient Virtual Machines Consolidation in Cloud Data Centers Using Reinforcement Learning. , 2014, , .		115
63	NeuroCGRA: A CGRA with support for neural networks. , 2014, , .		9
64	RuRot: Run-time rotatable-expandable partitions for efficient mapping in CGRAs. , 2014, , .		1
65	Efficient STDP Micro-Architecture for Silicon Spiking Neural Networks. , 2014, , .		2
66	Adjustable contiguity of run-time task allocation in networked many-core systems. , 2014, , .		27
67	Customizable Compression Architecture for Efficient Configuration in CGRAs. , 2014, , .		2
68	Exploring NoC jitter effect on simulation of spiking neural networks. , 2014, , .		0
69	Multi Rectangle Modeling Approach for Application Mapping on a Many-Core System. , 2014, , .		2
70	Integration of AES on Heterogeneous Many-Core System. , 2014, , .		3
71	Mixed-Criticality Run-Time Task Mapping for NoC-Based Many-Core Systems. , 2014, , .		17
72	Adaptive load balancing in learning-based approaches for many-core embedded systems. Journal of Supercomputing, 2014, 68, 1214-1234.	3.6	9

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73	Special section on advances in methods for adaptive multicore systems. Journal of Supercomputing, 2014, 68, 1023-1026.	3.6	0
74	Path-Based Partitioning Methods for 3D Networks-on-Chip with Minimal Adaptive Routing. IEEE Transactions on Computers, 2014, 63, 718-733.	3.4	60
75	Bi-LCQ: A low-weight clustering-based Q-learning approach for NoCs. Microprocessors and Microsystems, 2014, 38, 64-75.	2.8	17
76	Deadlock free routing algorithm for minimizing congestion in a Hamiltonian connected recursive 3D-NoCs. Microelectronics Journal, 2014, 45, 989-1000.	2.0	9
77	Positioning Antifragility for Clouds on Public Infrastructures. Procedia Computer Science, 2014, 32, 856-861.	2.0	5
78	High-Performance and Fault-Tolerant 3D NoC-Bus Hybrid Architecture Using ARB-NET-Based Adaptive Monitoring Platform. IEEE Transactions on Computers, 2014, 63, 734-747.	3.4	27
79	Digital column readout architectures for hybrid pixel detector readout chips. Journal of Instrumentation, 2014, 9, C01007-C01007.	1.2	6
80	Heterogeneous Parallelization of Aho-Corasick Algorithm. Advances in Intelligent Systems and Computing, 2014, , 153-160.	0.6	5
81	PDNOC: An Efficient Partially Diagonal Network-on-Chip Design. Lecture Notes in Computer Science, 2014, , 513-522.	1.3	1
82	Path-Based Multicast Routing for 2D and 3D Mesh Networks. , 2014, , 161-189.		0
83	Self-Adaptive SoCs for Dependability. Advances in Systems Analysis, Software Engineering, and High Performance Computing Book Series, 2014, , 1-21.	0.5	0
84	Hierarchical Agent-Based Monitoring Systems for Dynamic Reconfiguration in NoC Platforms. Advances in Systems Analysis, Software Engineering, and High Performance Computing Book Series, 2014, , 302-333.	0.5	0
85	High performance pattern matching on heterogeneous platform. Journal of Integrative Bioinformatics, 2014, 11, 253.	1.5	3
86	A systematic reordering mechanism for on-chip networks using efficient congestion-aware method. Journal of Systems Architecture, 2013, 59, 213-222.	4.3	10
87	Minimal-path fault-tolerant approach using connection-retaining structure in Networks-on-Chip. , 2013, , .		31
88	From traditional VLSI education to embedded electronics. , 2013, , .		1
89	LiRCUP: Linear Regression Based CPU Usage Prediction Algorithm for Live Migration of Virtual Machines in Data Centers. , 2013, , .		132
90	Mapping multiple applications with unbounded and bounded number of cores on many-core networks-on-chip. Microprocessors and Microsystems, 2013, 37, 460-471.	2.8	21

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91	Evaluate and optimize parallel Barnes-Hut algorithm for emerging many-core architectures. , 2013, , .		6
92	A multicore approach to model-based analysis and design of Cyber-Physical Systems. , 2013, , .		6
93	Enhanced fault-tolerant Network-on-Chip architecture using hierarchical agents. , 2013, , .		5
94	Energy Aware Consolidation Algorithm Based on K-Nearest Neighbor Regression for Cloud Data Centers. , 2013, , .		50
95	Energy-aware-task-parallelism for efficient dynamic voltage, and frequency scaling, in CGRAs. , 2013, , .		22
96	Implementation and evaluation of configuration scrubbing on CGRAs: A case study. , 2013, , .		0
97	Private configuration environments (PCE) for efficient reconfiguration, in CGRAs. , 2013, , .		7
98	FPGA implementation of AES-based crypto processor. , 2013, , .		13
99	Energy-aware coarse-grained reconfigurable architectures using dynamically reconfigurable isolation cells. , 2013, , .		22
100	Developing a power-efficient and low-cost 3D NoC using smart GALS-based vertical channels. Journal of Computer and System Sciences, 2013, 79, 440-456.	1.2	8
101	Cluster-based topologies for 3D Networks-on-Chip using advanced inter-layer bus architecture. Journal of Computer and System Sciences, 2013, 79, 475-491.	1.2	14
102	Formal approach to agent-based dynamic reconfiguration in Networks-On-Chip. Journal of Systems Architecture, 2013, 59, 709-728.	4.3	4
103	In-order delivery approach for 3D NoCs. , 2013, , .		0
104	Design and implementation of reconfigurable FIFOs for Voltage/Frequency Island-based Networks-on-Chip. Microprocessors and Microsystems, 2013, 37, 432-445.	2.8	11
105	Design space exploration of thermal-aware many-core systems. Journal of Systems Architecture, 2013, 59, 1197-1213.	4.3	1
106	Energy-aware fault-tolerant network-on-chips for addressing multiple traffic classes. Microprocessors and Microsystems, 2013, 37, 811-822.	2.8	8
107	High Performance Fault-Tolerant Routing Algorithm for NoC-Based Many-Core Systems. , 2013, , .		34
108	Enhancing Performance of 3D Interconnection Networks using Efficient Multicast Communication Protocol. , 2013, , .		4

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109	Optimal placement of vertical connections in 3D Network-on-Chip. Journal of Systems Architecture, 2013, 59, 441-454.	4.3	26
110	DyXYZ: Fully Adaptive Routing Algorithm for 3D NoCs. , 2013, , .		33
111	MD: Minimal path-based fault-tolerant routing in on-Chip Networks. , 2013, , .		41
112	Efficient application mapping in resource limited homogeneous NoC-based manycore systems. , 2013, , .		2
113	Towards a Configurable Many-core Accelerator for FPGA-based embedded systems. , 2013, , .		1
114	MMSoC. , 2013, , .		0
115	Smart hill climbing for agile dynamic mapping in many-core systems. , 2013, , .		72
116	Energy-Aware Fault-Tolerant CGRAs Addressing Application with Different Reliability Needs. , 2013, , .		12
117	Generation of Structural VHDL Code with Library Components from Formal Event-B Models. , 2013, , .		1
118	An efficient implementation of Hamiltonian path based multicast routing for 3D interconnection networks. , 2013, , .		3
119	Optimized multicore architectures for data parallel fast Fourier transform. , 2013, , .		2
120	OPTNOC: An Optimized 3D Network-on-Chip Design for Fast Memory Access. Lecture Notes in Computer Science, 2013, , 436-441.	1.3	0
121	t(k)-SA. , 2012, , .		7
122	A high-efficiency low-cost heterogeneous 3D network-on-chip design. , 2012, , .		12
123	Exploration of heuristic scheduling algorithms for 3D multicore processors. , 2012, , .		8
124	HIBS — Novel inter-layer bus structure for stacked architectures. , 2012, , .		10
125	CATRA- congestion aware trapezoid-based routing algorithm for on-chip networks. , 2012, , .		45
126	An efficient history-based routing algorithm for interconnection networks. , 2012, , .		1

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127	HLS-DoNoC: High-level simulator for dynamically organizational NoCs. , 2012, , .		1
128	Transport layer aware design of network interface in many-core systems. , 2012, , .		6
129	Status Data and Communication Aspects in Dynamically Clustered Network-on-Chip Monitoring. Journal of Electrical and Computer Engineering, 2012, 2012, 1-14.	0.9	0
130	Memory-efficient logic layer communication platform for 3D-stacked memory-on-processor architectures. , 2012, , .		1
131	Architectural modeling of pixel readout chips Velopix and Timepix3. Journal of Instrumentation, 2012, 7, C01093-C01093.	1.2	13
132	Partial-LastZ: An optimized hybridization technique for 3D NoC architecture enabling adaptive inter-layer communication. , 2012, , .		1
133	ARB-NET: A novel adaptive monitoring platform for stacked mesh 3D NoC architectures. , 2012, , .		11
134	NoC-AXI interface for FPGA-based MPSoC platforms. , 2012, , .		10
135	Power and Thermal Analysis of Stacked Mesh 3D NoC Using AdaptiveXYZ Routing Algorithm. , 2012, , .		2
136	Optimized Q-learning model for distributing traffic in on-Chip Networks. , 2012, , .		13
137	Dual Congestion Awareness scheme in On-Chip Networks. , 2012, , .		0
138	Energy-Aware Fault-Tolerant Network-on-Chips for Addressing Multiple Traffic Classes. , 2012, , .		6
139	Implementation and Analysis of Block Dense Matrix Decomposition on Network-on-Chips. , 2012, , .		3
140	GLB — Efficient Global Load Balancing method for moderating congestion in on-chip networks. , 2012, , .		3
141	Coarse and fine-grained monitoring and reconfiguration for energy-efficient NoCs. , 2012, , .		1
142	CoNA: Dynamic application mapping for congestion reduction in many-core systems. , 2012, , .		49
143	Semi-Serial On-Chip Link Implementation for Energy Efficiency and High Throughput. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2265-2277.	3.1	5
144	An Efficient Hybridization Scheme for Stacked Mesh 3D NoC Architecture. , 2012, , .		3

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145	Design and management of high-performance, reliable and thermal-aware 3D networks-on-chip. IET Circuits, Devices and Systems, 2012, 6, 308.	1.4	32
146	Thermal modeling and analysis of advanced 3D stacked structures. Procedia Engineering, 2012, 30, 248-257.	1.2	10
147	MAFA: Adaptive Fault-Tolerant Routing Algorithm for Networks-on-Chip. , 2012, , .		38
148	LEAR -- A Low-Weight and Highly Adaptive Routing Method for Distributing Congestions in On-chip Networks. , 2012, , .		22
149	Generic Monitoring and Management Infrastructure for 3D NoC-Bus Hybrid Architectures. , 2012, , .		9
150	Adaptive reinforcement learning method for networks-on-chip. , 2012, , .		23
151	HARAQ: Congestion-Aware Learning Model for Highly Adaptive Routing Algorithm in On-Chip Networks. , 2012, , .		74
152	PARS — An efficient congestion-Aware Routing method for Networks-on-Chip. , 2012, , .		11
153	Deadlock Free Routing Algorithm for Minimizing Data Packet Transmission in Network on Chip. International Journal of Embedded and Real-Time Communication Systems, 2012, 3, 70-81.	0.5	6
154	Memory-Efficient On-Chip Network With Adaptive Interfaces. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 146-159.	2.7	34
155	Parameter-Optimized Simulated Annealing for Application Mapping on Networks-on-Chip. Lecture Notes in Computer Science, 2012, , 307-322.	1.3	1
156	Adaptive Input-Output Selection Based On-Chip Router Architecture. Journal of Low Power Electronics, 2012, 8, 11-29.	0.6	25
157	Exploring a Low-Cost and Power-Efficient Hybridization Technique for 3D NoC-Bus Hybrid Architecture Using LastZ-Based Routing Algorithms. Journal of Low Power Electronics, 2012, 8, 403-414.	0.6	3
158	Survey of Self-Adaptive NoCs with Energy-Efficiency and Dependability. International Journal of Embedded and Real-Time Communication Systems, 2012, 3, 1-22.	0.5	4
159	An adaptive fuzzy logic-based routing algorithm for networks-on-chip. , 2011, , .		23
160	Compact generic intermediate representation (CGIR) to enable late binding in coarse grained reconfigurable architectures. , 2011, , .		21
161	High-performance on-chip network platform for memory-on-processor architectures. , 2011, , .		3
162	Exploring partitioning methods for 3D Networks-on-Chip utilizing adaptive routing model. , 2011, , .		25

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163	Thermal Analysis of Advanced 3D Stacked Systems. , 2011, , .		6
164	Efficient congestion-aware selection method for on-chip networks. , 2011, , .		2
165	Power-Efficient Inter-Layer Communication Architectures for 3D NoC. , 2011, , .		1
166	Agent-based on-chip network using efficient selection method. , 2011, , .		32
167	A Stacked Mesh 3D NoC Architecture Enabling Congestion-Aware and Reliable Inter-layer Communication. , 2011, , .		10
168	LastZ: An Ultra Optimized 3D Networks-on-Chip Architecture. , 2011, , .		12
169	A fault-tolerant and hierarchical routing algorithm for NoC architectures. , 2011, , .		4
170	Power and Area Optimization of 3D Networks-on-Chip Using Smart and Efficient Vertical Channels. Lecture Notes in Computer Science, 2011, , 278-287.	1.3	5
171	Exploring Congestion-Aware Methods for Distributing Traffic in On-Chip Networks. Communications in Computer and Information Science, 2011, , 319-327.	0.5	0
172	Q-learning based congestion-aware routing algorithm for on-chip network. , 2011, , .		54
173	Boosting performance of self-timed delay-insensitive bit parallel on-chip interconnects. IET Circuits, Devices and Systems, 2011, 5, 505.	1.4	5
174	A reconfigurable and adaptive routing method for fault-tolerant mesh-based networks-on-chip. AEU - International Journal of Electronics and Communications, 2011, 65, 630-640.	2.9	42
175	Cluster-based topologies for 3D stacked architectures. , 2011, , .		4
176	Congestion aware, fault tolerant, and thermally efficient inter-layer communication scheme for hybrid NoC-bus 3D architectures. , 2011, , .		42
177	Compression Based Efficient and Agile Configuration Mechanism for Coarse Grained Reconfigurable Architectures. , 2011, , .		16
178	Thermal Analysis of Job Allocation and Scheduling Schemes for 3D Stacked NoC's. , 2011, , .		2
179	Exploration of MPSoC monitoring and management systems. , 2011, , .		12
180	Analysis of Monitoring Structures for Network-on-Chip. International Journal of Embedded and Real-Time Communication Systems, 2011, 2, 49-67.	0.5	1

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181	Pipeline-based interlayer bus structure for 3D networks-on-chip. , 2010, , .		0
182	Efficient bytecode optimizations for a multicore Java co-processor system. , 2010, , .		4
183	Developing reconfigurable FIFOs to optimize power/performance of Voltage/Frequency Island-based networks-on-chip. , 2010, , .		2
184	Exploring a low-cost inter-layer communication scheme for 3D networks-on-chip. , 2010, , .		3
185	Heap access optimizations for a hardware-accelerated Java virtual machine. , 2010, , .		0
186	Process variation tolerant on-chip communication using receiver and driver reconfiguration. , 2010, , .		1
187	Monitoring and reconfiguration techniques for power supply variation tolerant on-chip links. , 2010, , .		0
188	Power and performance optimization of voltage/frequency island-based networks-on-chip using reconfigurable synchronous/bi-synchronous FIFOs. , 2010, , .		3
189	Input-Output Selection Based Router for Networks-on-Chip. , 2010, , .		8
190	CMIT — A novel cluster-based topology for 3D stacked architectures. , 2010, , .		5
191	A High-Performance Network Interface Architecture for NoCs Using Reorder Buffer Sharing. , 2010, , .		19
192	A Low-Latency and Memory-Efficient On-chip Network. , 2010, , .		24
193	Research and practices on 3D networks-on-chip architectures. , 2010, , .		27
194	High-Performance TSV Architecture for 3-D ICs. , 2010, , .		2
195	BBVC-3D-NoC: An Efficient 3D NoC Architecture Using Bidirectional Bisynchronous Vertical Channels. , 2010, , .		12
196	Tree-model based mapping for energy-efficient and low-latency Network-on-Chip. , 2010, , .		21
197	Self-Adaptive System for Addressing Permanent Errors in On-Chip Interconnects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 527-540.	3.1	74
198	A fault-tolerant and congestion-aware routing algorithm for Networks-on-Chip. , 2010, , .		23

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199	An efficient VFI-based NoC architecture using Johnson-encoded Reconfigurable FIFOs. , 2010, , .		5
200	An improved hardware acceleration scheme for Java method calls. , 2010, , .		0
201	Thermal modelling of 3D multicore systems in a flip-chip package. , 2010, , .		3
202	Hierarchical power monitoring on NoC - a case study for hierarchical agent monitoring design approach. , 2010, , .		3
203	Multi-application multi-step mapping method for many-core Network-on-Chips. , 2010, , .		7
204	Modeling Communication in Multiâ€“Processor Systemsâ€“onâ€“Chip Using Modular Connectors. International Journal of Embedded and Real-Time Communication Systems, 2010, 1, 23-44.	0.5	1
205	Hierarchical Agent Monitored Parallel On-Chip System. International Journal of Embedded and Real-Time Communication Systems, 2010, 1, 86-105.	0.5	7
206	Current Challenges in Embedded Communication Systems. International Journal of Embedded and Real-Time Communication Systems, 2010, 1, 1-21.	0.5	6
207	An efficent dynamic multicast routing protocol for distributing traffic in NOCs. , 2009, , .		18
208	Efficient execution of switch instructions on a multicore Java co-processor system. , 2009, , .		1
209	High-speed completion detection for current sensing on-chip interconnects. Electronics Letters, 2009, 45, 547.	1.0	4
210	Fault tolerant distributed routing algorithms for mesh Networks-on-Chip. , 2009, , .		6
211	Multi network interface architectures for fault tolerant Network-on-Chip. , 2009, , .		6
212	Multi-dimensional routing algorithms for congestion minimization in Network-on-Chip. , 2009, , .		0
213	Self-timed thermal sensing and monitoring of multicore systems. , 2009, , .		6
214	Thermal analysis of on-chip interconnects in multicore systems. , 2009, , .		0
215	Power Aware System Refinement. Electronic Notes in Theoretical Computer Science, 2008, 201, 223-253.	0.9	2
216	On-line Distributed Thermal Sensing and Monitoring of Multicore Systems. , 2008, , .		3

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217	Instruction Set Enhancements for High-Performance Multicore Execution on the REALJava Platform. , 2008, , .		6
218	Area efficient delay-insensitive and differential current sensing on-chip interconnect. , 2008, , .		2
219	A novel hardware acceleration scheme for java method calls. , 2008, , .		3
220	Distributed Traffic Monitoring Methods for Adaptive Network-on-Chip. , 2008, , .		4
221	Current Mode On-Chip Interconnect using Level-Encoded Two-Phase Dual-Rail Encoding. , 2007, , .		3
222	Fault Tolerance Analysis of NoC Architectures. , 2007, , .		23
223	FPGA Prototype of the REALJava Co-Processor. , 2007, , .		2
224	High-Performance Long NoC Link Using Delay-Insensitive Current-Mode Signaling. VLSI Design, 2007, 2007, 1-13.	0.5	19
225	Online Reconfigurable Self-Timed Links for Fault Tolerant NoC. VLSI Design, 2007, 2007, 1-13.	0.5	80
226	Time Aware System Refinement. Electronic Notes in Theoretical Computer Science, 2007, 187, 91-106.	0.9	4
227	Java Co-Processor for Embedded Systems. , 2007, , 287-308.		7
228	Fault-tolerant Routing Approach for Reconfigurable Networks-on-Chip. , 2006, , .		9
229	Analysis of Crosstalk and Process Variations Effects on On-Chip Interconnects. , 2006, , .		2
230	Implementing a Self-Timed Low-Power Java Accelerator for Network-on-Chip Applications. , 2006, , .		0
231	Comparative Study of Synthesis for Asynchronous and Synchronous Cache Controllers. , 2006, , .		2
232	Formal Modelling of Multiclocked SoC Systems. , 2006, , .		0
233	Combination Selection Counter for Gaussian Distribution Applications. Midwest Symposium on Circuits and Systems, 2006, , .	1.0	5
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