Narasimhulu Thoti

List of Publications by Year
in descending order

21	162	1307594 7	1281871 11
papers	citations	h-index	g-index

21	21	21	35
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Gateâ€allâ€around nanowire vertical tunneling FETs by ferroelectric internal voltage amplification. Nanotechnology, 2022, 33, 055201.	2.6	10
2	Significance of Work Function Fluctuations in SiGe/Si Hetero-Nanosheet Tunnel-FET at Sub-3 nm Nodes. IEEE Transactions on Electron Devices, 2022, 69, 434-438.	3.0	14
3	Device-Simulation-Based Machine Learning Technique for the Characteristic of Line Tunnel Field-Effect Transistors. IEEE Access, 2022, 10, 53098-53107.	4.2	2
4	Design of GAA Nanosheet Ferroelectric Area Tunneling FET and Its Significance with DC/RF Characteristics Including Linearity Analyses. Nanoscale Research Letters, 2022, 17, 53.	5.7	8
5	Machine Learning Approach to Predicting Tunnel Field-Effect Transistors. , 2021, , .		3
6	p-SiGe nanosheet line tunnel field-effect transistors with ample exploitation of ferroelectric. Japanese Journal of Applied Physics, 2021, 60, 054001.	1.5	7
7	A Novel Design of Ferroelectric Nanowire Tunnel Field Effect Transistors. , 2021, , .		1
8	Promised Design of Energy-Efficient Negative-Capacitance Vertical Tunneling FET. ECS Journal of Solid State Science and Technology, 2021, 10, 075002.	1.8	8
9	Random telegraph noise in gate-all-around silicon nanowire MOSFETs induced by a single charge trap or random interface traps. Journal of Computational Electronics, 2020, 19, 253-262.	2.5	14
10	Effects of a dual spacer on electrical characteristics and random telegraph noise of gate-all-around silicon nanowire p-type metalâ€“oxideâ€“semiconductor field-effect transistors. Japanese Journal of Applied Physics, 2020, 59, SGGA02.	1.5	7
11	Scaling Limitations of Line TFETs at Sub-8-nm Technology Node. , 2020, , .		5
12	Effects of Spacer and Single-Charge Trap on Voltage Transfer Characteristics of Gate-All-Around Silicon Nanowire CMOS Devices and Circuits. , 2020, , .		11
13	New Proficient Ferroelectric Nanosheet Line Tunneling FETs with Strained SiGe through Scaled n-epitaxial Layer. , 2020, , .		5
14	Influence of Fringing-Field on DC/AC Characteristics of Siâ,ê‹â„“Geâ„“ Based Multi-Channel Tunnel FETs. IEEE Access, 2020, 8, 208658-208668.	4.2	16
15	Optimal Inter-Gate Separation and Overlapped Source of Multi-Channel Line Tunnel FETs. IEEE Open Journal of Nanotechnology, 2020, 1, 38-46.	2.0	16
16	High-Performance Metal-Ferroeletric-Semiconductor Nanosheet Line Tunneling Field Effect Transistors with Strained SiGe. , 2020, , .		6
17	Characteristics of Gate-All-Around Silicon Nanowire and Nanosheet MOSFETs with Various Spacers. , 2020, , .		13
18	Comparative investigation of Si/Sio.6Geo.4/InAs 3D-fin-TFET for its optimized performance. , 2018, , .		0

#	Article	IF	Citations
19	Investigation of optimized Si<inf>1-x</inf>Ge<inf>x</inf> 3D-fin-TFET by varying the fin height. , 2018, , .		0
20	Performance metrics estimation in IC process flow by using TCAD simulations. TEPEXI BoletÃn CientÃfico De La Escuela Superior Tepeji Del RÃo, 2018, 5, .	0.0	0
21	RF performance enhancement in multi-fin TFETs by scaling inter fin separation. Materials Science in Semiconductor Processing, 2017, 71, 304-309.	4.0	16