John Kim

List of Publications by Year
in descending order

81 papers	3,697 citations	759233 12 h-index	610901 24 g-index
81 all docs	81 docs citations	81 times ranked	1436 citing authors

#	Article	IF	Citations
1	A software-defined tensor streaming multiprocessor for large-scale machine learning. , 2022, , .		6
2	Dynamic global adaptive routing in high-radix networks. , 2022, , .		2
3	BTS. , 2022, , .		37
4	The Case for Dynamic Bias in Global Adaptive Routing. IEEE Computer Architecture Letters, 2021, 20, 38-41.	1.5	2
5	BoomGate: Deadlock Avoidance in Non-Minimal Routing for High-Radix Networks. , 2021, , .		4
6	GNNMark: A Benchmark Suite to Characterize Graph Neural Network Training on GPUs. , 2021, , .		15
7	Ghost Routing to Enable Oblivious Computation on Memory-centric Networks. , 2021, , .		1
8	Decoupled SSD: Reducing Data Movement on NAND-Based Flash SSD. IEEE Computer Architecture Letters, 2021, 20, 150-153.	1.5	4
9	Network-on-Chip Microarchitecture-based Covert Channel in GPUs. , 2021, , .		7
10	Navigator: Dynamic Multi-kernel Scheduling to Improve GPU Performance. , 2020, , .		4
11	Griffin: Hardware-Software Support for Efficient Page Migration in Multi-GPU Systems. , 2020, , .		19
12	Valkyrie. , 2020, , .		11
13	MGPUSim. , 2019, , .		49
14	Ghost routers. , 2019, , .		0
15	DeepHiR. , 2019, , .		3
16	A Novel Covert Channel Attack Using Memory Encryption Engine Cache. , 2019, , .		3
17	A Case for Software-Based Adaptive Routing in NUMA Systems. , 2019, , .		2
18	Enforcing Last-Level Cache Partitioning through Memory Virtual Channels. , 2019, , .		3

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19	Practical and efficient incremental adaptive routing for HyperX networks. , 2019, , .		9
20	Multi-dimensional Parallel Training of Winograd Layer on Memory-Centric Architecture. , 2018, , .		10
21	Profiling DNN Workloads on a Volta-based DGX-1 System. , 2018, , .		22
22	Footprint. Computer Architecture News, 2017, 45, 691-702.	2.5	6
23	Footprint. , 2017, , .		14
24	History-Based Arbitration for Fairness in Processor-Interconnect of NUMA Servers. Computer Architecture News, 2017, 45, 765-777.	2.5	2
25	Evaluation of Performance Unfairness in NUMA System Architecture. IEEE Computer Architecture Letters, 2017, 16, 26-29.	1.5	7
26	History-Based Arbitration for Fairness in Processor-Interconnect of NUMA Servers. , 2017, , .		3
27	History-Based Arbitration for Fairness in Processor-Interconnect of NUMA Servers. Operating Systems Review (ACM), 2017, 51, 765-777.	1.9	1
28	History-Based Arbitration for Fairness in Processor-Interconnect of NUMA Servers. ACM SIGPLAN Notices, 2017, 52, 765-777.	0.2	0
29	Adaptive and flexible key-value stores through soft data partitioning. , 2016, , .		2
30	UMH. Transactions on Architecture and Code Optimization, 2016, 13, 1-25.	2.0	16
31	Contention-based congestion management in large-scale networks. , 2016, , .		17
32	Accelerating Linked-list Traversal Through Near-Data Processing. , 2016, , .		26
33	Design and Analysis of Hybrid Flow Control for Hierarchical Ring Network-on-Chip. IEEE Transactions on Computers, 2016, 65, 480-494.	3.4	8
34	Overcoming far-end congestion in large-scale networks. , 2015, , .		43
35	Multi-GPU System Design with Memory Networks. , 2014, , .		40
36	Security Vulnerability in Processor-Interconnect Router Design. , 2014, , .		5

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37	Low-Overhead Network-on-Chip Support for Location-Oblivious Task Placement. IEEE Transactions on Computers, 2014, 63, 1487-1500.	3.4	13
38	Extending bufferless on-chip networks to high-throughput workloads. , 2014, , .		8
39	Transportation-network-inspired network-on-chip. , 2014, , .		13
40	Mutually Aware Prefetcher and On-Chip Network Designs for Multi-Cores. IEEE Transactions on Computers, 2014, 63, 2316-2329.	3.4	4
41	A detailed and flexible cycle-accurate Network-on-Chip simulator. , 2013, , .		504
42	Clumsy Flow Control for High-Throughput Bufferless On-Chip Networks. IEEE Computer Architecture Letters, 2013, 12, 47-50.	1.5	22
43	Memory-centric system interconnect design with Hybrid Memory Cubes. , 2013, , .		9
44	Scalable high-radix router microarchitecture using a network switch organization. Transactions on Architecture and Code Optimization, 2013, 10, 1-25.	2.0	7
45	Scheduling in Heterogeneous Computing Environments for Proximity Queries. IEEE Transactions on Visualization and Computer Graphics, 2013, 19, 1513-1525.	4.4	7
46	Designing on-chip networks for throughput accelerators. Transactions on Architecture and Code Optimization, 2013, 10, 1-35.	2.0	8
47	Guest Editorial New Interconnect Technologies in On-Chip Communication. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 121-123.	3.6	0
48	Exploiting New Interconnect Technologies in On-Chip Communication. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 124-136.	3.6	30
49	Providing cost-effective on-chip network bandwidth in GPGPUs. , 2012, , .		30
50	Scalable on-chip network in power constrained manycore processors. , 2012, , .		2
51	Network within a network approach to create a scalable high-radix router microarchitecture. , 2012, , .		19
52	Leveraging torus topology with deadlock recovery for cost-efficient on-chip network. , 2011, , .		7
53	An Alternative Memory Access Scheduling in Manycore Accelerators. , 2011, , .		5
54	FeatherWeight. , 2011, , .		22

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55	Exploiting Mutual Awareness between Prefetchers and On-chip Networks in Multi-cores. , 2011, , .		3
56	High Performance Datacenter Networks: Architectures, Algorithms, and Opportunities. Synthesis Lectures on Computer Architecture, 2011, 6, 1-115.	1.3	22
57	Energy-Aware On-Chip Networks. , 2011, , 93-118.		0
58	On-Chip Network Evaluation Framework. , 2010, , .		9
59	Probabilistic Distance-Based Arbitration: Providing Equality of Service for Many-Core CMPs. , 2010, , .		37
60	FlexiShare: Channel sharing for an energy-efficient nanophotonic crossbar. , 2010, , .		144
61	Throughput-Effective On-Chip Networks for Manycore Accelerators. , 2010, , .		111
62	Indirect adaptive routing on large scale interconnection networks. Computer Architecture News, 2009, 37, 220-231.	2.5	25
63	Exploring concentration and channel slicing in on-chip network router. , 2009, , .		46
64	Firefly. Computer Architecture News, 2009, 37, 429-440.	2.5	85
65	Router microarchitecture and scalability of ring topology in on-chip networks. , 2009, , .		32
66	HPCCD: Hybrid Parallel Continuous Collision Detection using CPUs and GPUs. Computer Graphics Forum, 2009, 28, 1791-1800.	3.0	57
67	Low-cost router microarchitecture for on-chip networks. , 2009, , .		127
68	Indirect adaptive routing on large scale interconnection networks. , 2009, , .		79
69	Firefly. , 2009, , .		259
70	Cost-Efficient Dragonfly Topology for Large-Scale Systems. IEEE Micro, 2009, 29, 33-40.	1.8	55
71	Achieving predictable performance through better memory controller placement in many-core CMPs. , 2009, , .		105
72	Technology-Driven, Highly-Scalable Dragonfly Topology. , 2008, , .		380

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73	Technology-Driven, Highly-Scalable Dragonfly Topology. Computer Architecture News, 2008, 36, 77-88.	2.5	219
74	Flattened butterfly. Computer Architecture News, 2007, 35, 126-137.	2.5	93
75	Flattened butterfly. , 2007, , .		273
76	Flattened Butterfly Topology for On-Chip Networks. , 2007, , .		203
77	Flattened Butterfly Topology for On-Chip Networks. IEEE Computer Architecture Letters, 2007, 6, 37-40.	1.5	61
78	Flattened Butterfly Topology for On-Chip Networks. Microarchitecture (MICRO), Proceedings of the Annual International Symposium on, 2007, , .	0.0	0
79	Interconnect routing and scheduling---Adaptive routing in high-radix clos network. , 2006, , .		37
80	Adaptive Routing in High-Radix Clos Network. , 2006, , .		40
81	Microarchitecture of a High-Radix Router. Computer Architecture News, 2005, 33, 420-431.	2.5	82