Fayez Gebali

List of Publications by Year
in descending order

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100 papers	1,190 citations	516710 16 h-index	501196 28 g-index
108 all docs	108 docs citations	108 times ranked	927 citing authors

#	Article	IF	Citations
1	Low-Space Bit-Parallel Systolic Structure for AOP-Based Multiplier Suitable for Resource-Constrained IoT Edge Devices. Mathematics, 2022, 10, 815.	2.2	0
2	A Novel Framework for Combining Multiple Radar Waveforms Using Time Compression Overlap-Add. IEEE Transactions on Signal Processing, 2021, 69, 4371-4384.	5.3	2
3	A Novel Intrusion Detection System for RPL-Based Cyberâ€“Physical Systems. Canadian Journal of Electrical and Computer Engineering, 2021, 44, 246-252.	2.0	17
4	Compact Bit-Parallel Systolic Multiplier Over GF(2 m). Canadian Journal of Electrical and Computer Engineering, 2021, 44, 199-205.	2.0	2
5	Expanding Window Dynamic-Programming-Based Track-Before-Detect With Order Statistics in Weibull Distributed Clutter. IEEE Transactions on Aerospace and Electronic Systems, 2020, 56, 2564-2575.	4.7	23
6	Implementation of Ultrahigh-Speed Decimators. Canadian Journal of Electrical and Computer Engineering, 2020, 43, 310-314.	2.0	0
7	Detecting Misleading Information on COVID-19. IEEE Access, 2020, 8, 165201-165215.	4.2	100
8	Performance Analysis of Multiuser FSO/RF Network Under Non-Equal Priority With P -Persistence Protocol. IEEE Transactions on Wireless Communications, 2020, 19, 1802-1813.	9.2	4
9	Parallel Multidimensional Lookahead Sorting Algorithm. IEEE Access, 2019, 7, 75446-75463.	4.2	6
10	High Speed and Low Area Complexity Extended Euclidean Inversion Over Binary Fields. IEEE Transactions on Consumer Electronics, 2019, 65, 408-417.	3.6	5
11	Linear Processor Array Architectures for Similarity Distance Computation. , 2019, , .		0
12	Low-Complexity Scalable Architectures for Parallel Computation of Similarity Measures. Scientific Programming, 2019, 2019, 1-11.	0.7	0
13	Fast Large Integer Modular Addition in GF(p) Using Novel Attribute-Based Representation. IEEE Access, 2019, 7, 58704-58719.	4.2	4
14	A Novel Smeared Synthesized LFM TC-OLA Radar System: Design and Performance Evaluation. IEEE Access, 2019, 7, 18574-18589.	4.2	5
15	Hardware Trojan Detection Using Reconfigurable Assertion Checkers. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1575-1586.	3.1	10
16	Handover Optimization and User Mobility Prediction in LTE Femtocells Network. , 2019, , .		12
17	High Performance Implementation of Nested Array Beamformer for Wideband Radar Applications. , 2019, , .		0
18	Decimator systolic arrays design space exploration for multirate signal processing applications. IET Circuits, Devices and Systems, 2019, 13, 1232-1240.	1.4	1

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19	Simulating Attacks for RPL and Generating Multi-class Dataset for Supervised Machine Learning. , 2019, , .		15
20	Systolic array design space exploration of interpolators for multiâ€rate systems. IET Circuits, Devices and Systems, 2019, 13, 1032-1038.	1.4	1
21	Multi-Core Dataflow Design and Implementation of Secure Hash Algorithm-3. IEEE Access, 2018, 6, 6092-6102.	4.2	9
22	New systolic array architecture for finite field division. IEICE Electronics Express, 2018, 15, 20180255-20180255.	0.8	19
23	Design Space Exploration of 2-D Processor Array Architectures for Similarity Distance Computation. IEEE Transactions on Parallel and Distributed Systems, 2017, 28, 2218-2228.	5.6	3
24	Programmable assertion checkers for hardware Trojan detection. , 2017, , .		4
25	Cross Layer Analysis of P2MP Hybrid FSO/RF Network. Journal of Optical Communications and Networking, 2017, 9, 234.	4.8	14
26	Scalable and Unified Digit-Serial Processor Array Architecture for Multiplication and Inversion Over GF(2^{m}). IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2894-2906.	5.4	28
27	Systolic design space exploration of polynomial division over GF(m2). , 2017, , .		2
28	On Time Compression Overlap-Add Technique in Linear Frequency Modulation Pulse Compression Radar Systems: Design and Performance Evaluation. IEEE Access, 2017, 5, 27525-27537.	4.2	11
29	Complex event processing enrichment: Motivations and challenges. , 2017, , .		1
30	Data-flow implementation of concurrent asynchronous systems. , 2017, , .		0
31	Enhancement of time compression overlap-add using multirate downsample upsample shift add algorithm. , 2017, , .		3
32	Performance evaluation of time compression overlap-add radar systems based on order-statistics CFAR under convolution noise jamming. , 2017, , .		5
33	A New Characterization of Hardware Trojans. IEEE Access, 2016, 4, 2721-2731.	4.2	24
34	Efficient Scalable Digit-Serial Inverter Over GF(2^{m}) for Ultra-Low Power Devices. IEEE Access, 2016, 4, 9758-9763.	4.2	5
35	Optimal Design of Dual-Hop VLC/RF Communication System With Energy Harvesting. IEEE Communications Letters, 2016, 20, 1979-1982.	4.1	102
36	Hardware Covert Attacks and Countermeasures. , 2016, , .		3

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37	Hardware attacks: an algebraic approach. Journal of Cryptographic Engineering, 2016, 6, 325-337.	1.8	4
38	Classification of hardware trojan detection techniques. , 2015, , .		12
39	Hardware attack risk assessment. , 2015, , .		3
40	Teaching engineering design in a four-course sequence. , 2015, , .		3
41	Review of Elliptic Curve Processor architectures. , 2015, , .		4
42	An attribute based classification of hardware trojans. , 2015, , .		9
43	Performance analysis of 64-bit Carry Lookahead Adders using conventional and hierarchical structure styles. , 2015, , .		5
44	Ship detection and property extraction in radar images using hardware. , 2015, , .		0
45	CRT based somewhat homomorphic encryption over the integers. , 2015, , .		0
46	Optimized structures of hybrid ripple carry and hierarchical carry lookahead adders. Microelectronics Journal, 2015, 46, 783-794.	2.0	16
47	Outage Analysis of Practical FSO/RF Hybrid System With Adaptive Combining. IEEE Communications Letters, 2015, 19, 1366-1369.	4.1	100
48	Power Adaptation Based on Truncated Channel Inversion for Hybrid FSO/RF Transmission With Adaptive Combining. IEEE Photonics Journal, 2015, 7, 1-12.	2.0	29
49	Systolic Array Architectures for Sunarâ€“KoÃ§ Optimal Normal Basis Type II Multiplier. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2090-2102.	3.1	17
50	Efficient Scalable Serial Multiplier Over GF(<inline-formula> <tex-math) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50 227 Td (notation="on Trinomial. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2322-2326.	3.1	24
51	Simulations and performance evaluation of Real-Time Multi-core Systems. , 2014, , .		0
52	NFC security analysis and vulnerabilities in healthcare applications. , 2013, , .		18
53	PCBSecure: A new software tool to evaluate the security of Printed Circuit Boards. , 2013, , .		0
54	Unified multiâ€objective mapping and architecture customisation of networksâ€onâ€chip. IET Computers and Digital Techniques, 2013, 7, 282-293.	1.2	23

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55	Capstone team design projects in engineering curriculum: Content and management. , 2012, , .		4
56	DominoMAC: A Wireless Sensor Networks Medium Access Protocol. , 2012, , .		1
57	GPS Waypoint Application. , 2012, , .		6
58	DSDMAC: Dual Sensing Directional MAC Protocol for Ad Hoc Networks with Directional Antennas. IEEE Transactions on Vehicular Technology, 2012, 61, 1266-1275.	6.3	58
59	New processor array architecture for scalable radix 8 montgomery modular multiplication algorithm. , 2011, , .		2
60	Processor Array Architectures for Scalable Radix 4 Montgomery Modular Multiplication Algorithm. IEEE Transactions on Parallel and Distributed Systems, 2011, 22, 1142-1149.	5.6	14
61	Floating-point adaptive CORDIC (FPA-CORDIC) algorithm for elementary function calculation. , 2011, , .		0
62	Improving Networksâ€onâ€Chip performability: A topologyâ€based approach. International Journal of Circuit Theory and Applications, 2011, 39, 557-572.	2.0	6
63	Finite Field Multiplication Using Reordered Normal Basis Multiplier. , 2011, , .		1
64	Networks-on-chip topology optimization subject to power, delay, and reliability constraints. , 2010, , .		8
65	Multi-objective optimization for Networks-on-Chip architectures using Genetic Algorithms. , 2010, , .		20
66	Multi-objective optimization of NoC standard architectures using Genetic Algorithms. , 2010, , .		2
67	Enhanced Busy-Tone-Assisted MAC Protocol for Wireless Ad Hoc Networks. , 2010, , .		3
68	Analytical modelling and performance analysis forwireless ad-hoc networks using four-way handshaking mechanism. , 2009, , .		1
69	Cross-layer analysis of wireless LANS: Backoff strategies and error control. , 2009, , .		0
70	Area-aware topology generation for Application-Specific Networks-on-Chip using network partitioning. , 2009, , .		6
71	Power optimization for application-specific networks-on-chips: A topology-based approach. Microprocessors and Microsystems, 2009, 33, 343-355.	2.8	31
72	High-performance, low-power architecture for scalable radix 2 montgomery modular multiplication algorithm. Canadian Journal of Electrical and Computer Engineering, 2009, 34, 152-157.	2.0	18

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73	Modeling the Throughput and Delay in Wireless Multihop Ad Hoc Networks. , 2009, , .		15
74	Methodologies for data mining and modeling of atmospheric pollutants. , 2009, , .		0
75	A delay-aware topology-based design for Networks-on-Chip applications. , 2009, , .		8
76	Area and delay optimization for Networks-on-Chip architectures using Genetic Algorithms. , 2009, , .		1
77	Cross-Layer Modeling of Wireless Ad Hoc Networks in the Presence of Channel Noise. , 2009, , .		0
78	Prioritized eâ€mail servicing to reduce nonâ€spam delay and loss: A performance analysis. International Journal of Network Management, 2008, 18, 325-344.	2.2	5
79	Networks-on-Chip topology generation techniques: Area and delay evaluation. , 2008, , .		5
80	Corrections to “Design and Performance Analysis of a Unified, Reconfigurable HMAC-Hash Unit” [Dec 07 2683-2695]. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2008, 55, 708-708.	0.1	0
81	Power-aware topology optimization for networks-on-chips. , 2008, , .		17
82	Quality of service support in wireless local area network with error control protocol. , 2008, , .		1
83	Backoff Strategies in Hiperlan with Error Control Protocol. , 2008, , .		2
84	Analysis of Computer and Communication Networks. , 2008, , .		59
85	Scheduling Algorithms. , 2008, , 1-45.		1
86	Interconnection Networks. , 2008, , 1-43.		0
87	Queuing Analysis. , 2008, , 1-46.		0
88	Performance Analysis of Server-Side Spam Control Strategies Based on Layer-3 Classification. , 2007, , .		2
89	Rejecting Spam during SMTP Sessions. , 2007, , .		1
90	A Reservation-Based Multiple Access Protocol for OFDMA Networks with Adaptive Backoff Strategy. , 2007, , .		3

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91	Performance Analysis of the IEEE 802.11 DCF. , 2007, , .		4
92	A Topology-based Design Methodology for Networks-on-Chip Applications. , 2007, , .		20
93	Introducing OperaNP: A Reconfigurable NoC-Based Platform. , 2007, , .		5
94	A new analytical model for computing blocking probability in optical burst switching networks. IEEE Journal on Selected Areas in Communications, 2006, 24, 120-128.	14.0	31
95	Distributed Layer-3 E-Mail Classification for Spam Control. , 2006, , .		6
96	Design Space Exploration of a Reconfigurable HMAC-Hash Unit. , 2006, , .		1
97	A hierarchical design methodology for full-search block matching motion estimation. Multidimensional Systems and Signal Processing, 2006, 17, 327-341.	2.6	5
98	Designing an HMAC-Hash Unit on FPGAs Using Handel-C. , 2006, , .		0
99	A Delay Model for Networks-on-Chip Output-Queuing Router. , 2006, , .		6
100	A fast string search algorithm for deep packet classification. Computer Communications, 2004, 27, 1524-1538.	5.1	22