Francesco Centurelli

List of Publications by Year
in descending order

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108	692	567144	752573
papers	citations	15 h-index	20 g-index

108	108	108	291
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A SiGe HBT 6th-Order 10 GHz Inductor-Less Anti-Aliasing Low-Pass Filter for High-Speed ATI Digitizers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 100-113.	3.5	5
2	An Ultra-Low-Voltage class-AB OTA exploiting local CMFB and Body-to-Gate interface. AEU - International Journal of Electronics and Communications, 2022, 145, 154081.	1.7	14
3	General Approach to the Calibration of Innovative MFP Multichannel Digitizers. IEEE Transactions on Instrumentation and Measurement, 2022, 71, 1-14.	2.4	3
4	A Biasing Approach to Design Ultra-Low-Power Standard-Cell-Based Analog Building Blocks for Nanometer SoCs. IEEE Access, 2022, 10, 25892-25900.	2.6	11
5	A Tree-Based Architecture for High-Performance Ultra-Low-Voltage Amplifiers. Journal of Low Power Electronics and Applications, 2022, 12, 12.	1.3	17
6	A New Fully Closed-Loop, High-Precision, Class-AB CCII for Differential Capacitive Sensor Interfaces. Electronics (Switzerland), 2022, 11, 903.	1.8	1
7	80ÂdB tuning range transimpedance amplifier exploiting the Switched-Resistor approach. AEU - International Journal of Electronics and Communications, 2022, 149, 154196.	1.7	4
8	A Standard-Cell-Based CMFB for Fully Synthesizable OTAs. Journal of Low Power Electronics and Applications, 2022, 12, 27.	1.3	15
9	Sub-Î¼W Front-End Low Noise Amplifier for Neural Recording Applications. , 2022, , .		3
10	High-efficiency 0.3V OTA in CMOS 130nm technology using current mirrors with gain. , 2022, , .		3
11	Design of Low-Voltage Power Efficient Frequency Dividers in Folded MOS Current Mode Logic. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 680-691.	3.5	8
12	A 0.3 V, Rail-to-Rail, Ultralow-Power, Non-Tailed, Body-Driven, Sub-Threshold Amplifier. Applied Sciences (Switzerland), 2021, 11, 2528.	1.3	23
13	A 0.3 V Rail-to-Rail Ultra-Low-Power OTA with Improved Bandwidth and Slew Rate. Journal of Low Power Electronics and Applications, 2021, 11, 19.	1.3	22
14	A Very-Low-Voltage Frequency Divider in Folded MOS Current Mode Logic With Complementary n- and p-type Flip-Flops. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 998-1008.	2.1	10
15	A Low-Voltage High-Performance Frequency Divider exploiting Folded MCML. , 2021, , .		1
16	0.5-V Frequency Dividers in Folded MCML Exploiting Forward Body Bias: Analysis and Comparison. Electronics (Switzerland), 2021, 10, 1383.	1.8	2
17	A New VCII Application: Sinusoidal Oscillators. Journal of Low Power Electronics and Applications, 2021, 11, 30.	1.3	13
18	A Novel OTA Architecture Exploiting Current Gain Stages to Boost Bandwidth and Slew-Rate. Electronics (Switzerland), 2021, 10, 1638.	1.8	13

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19	Distributed switched-resistor approach for high-Q biquad filters. AEU - International Journal of Electronics and Communications, 2021, 138, 153894.	1.7	5
20	Compact E-Band I/Q Receiver in SiGe BiCMOS for 5G Backhauling Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3098-3102.	2.2	9
21	An E-band Variable Gain Amplifier with 24ÂdB-control range and 80 to 100ÂGHz 1ÂdB bandwidth in SiGe BiCMOS technology. Frequenz, 2021, .	0.6	1
22	A class-AB linear transconductor with enhanced linearity. AEU - International Journal of Electronics and Communications, 2021, 140, 153955.	1.7	5
23	A Detailed Model of the Switched-Resistor Technique. IEEE Open Journal of Circuits and Systems, 2021, 2, 497-507.	1.4	2
24	0.6â€V CMOS cascode OTA with complementary gateâ€driven gainâ€boosting and forward body bias. International Journal of Circuit Theory and Applications, 2020, 48, 15-27.	1.3	22
25	Low power switched-resistor band-pass filter for neural recording channels in 130nm CMOS. Heliyon, 2020, 6, e04723.	1.4	10
26	A Power Efficient Frequency Divider With 55 GHz Self-Oscillating Frequency in SiGe BiCMOS. Electronics (Switzerland), 2020, 9, 1968.	1.8	5
27	A low-voltage class-AB OTA exploiting adaptive biasing. AEU - International Journal of Electronics and Communications, 2020, 122, 153282.	1.7	10
28	An improved reversed miller compensation technique for threeâ€stage CMOS OTAs with double poleâ€zero cancellation and almost singleâ€pole frequency response. International Journal of Circuit Theory and Applications, 2020, 48, 1990-2005.	1.3	4
29	Delay models and design guidelines for MCML gates with resistor or PMOS load. Microelectronics Journal, 2020, 99, 104755.	1.1	7
30	Lowâ€power classâ€AB 4thâ€order lowâ€pass filter based on current conveyors with dynamic mismatch compensation of biasing errors. International Journal of Circuit Theory and Applications, 2020, 48, 472-484.	1.3	1
31	10-GHz Fully Differential Sallenâ€“Key Lowpass Biquad Filters in 55nm SiGe BiCMOS Technology. Electronics (Switzerland), 2020, 9, 563.	1.8	4
32	A revision of the theory of THz detection by MOSFET in the light of the self-mixing model. , 2020, , .		0
33	A revision of the theory of THz detection by MOS-FET in the light of the self-mixing model in the substrate. , 2020, , .		0
34	CMOS integrated system for Terahertz Detection. , 2020, , .		0
35	Highâ€gain, highâ€CMRR class AB operational transconductance amplifier based on the flipped voltage follower. International Journal of Circuit Theory and Applications, 2019, 47, 499-512.	1.3	9
36	A low-power class-AB Gm-C biquad stage in CMOS 40nm technology. , 2019, , .		1

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37	A Topology of Fully Differential Class-AB Symmetrical OTA With Improved CMRR. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1504-1508.	2.2	19
38	A 10â€‰GHz inductorless active SiGe HBT lowpass filter. International Journal of RF and Microwave Computer-Aided Engineering, 2018, 28, e21567.	0.8	6
39	A 0.6 V classâ€AB railâ€toâ€rail CMOS OTA exploiting threshold lowering. Electronics Letters, 2018, 54, 930-932.	0.5	16
40	Low power DDA-based instrumentation amplifier for neural recording applications in 65â€¯nm CMOS. AEU - International Journal of Electronics and Communications, 2018, 92, 30-35.	1.7	26
41	Fully Differential Class-AB OTA with Improved CMRR. Journal of Circuits, Systems and Computers, 2017, 26, 1750169.	1.0	1
42	The AB-CCII, a novel adaptive biasing LV-LP current conveyor architecture. AEU - International Journal of Electronics and Communications, 2017, 79, 301-306.	1.7	10
43	Reconfigurable low voltage inverter-based sample-and-hold amplifier. , 2017, , .		2
44	A fully-differential class-AB OTA with CMRR improved by local feedback. , 2017, , .		3
45	Power-efficient dynamic-biased CCII. , 2017, , .		3
46	On the use of voltage conveyors for the synthesis of biquad filters and arbitrary networks. , 2017, , .		9
47	Class-AB current conveyors based on the FVF. , 2017, , .		4
48	Comparative performance analysis and complementary triode based CMFB circuits for fully differential class AB symmetrical OTAs with low power consumption. International Journal of Circuit Theory and Applications, 2016, 44, 1039-1054.	1.3	18
49	Blind and reference channel-based time interleaved ADC calibration schemes: a comparison. Proceedings of SPIE, 2016, , .	0.8	1
50	A new class-AB Flipped Voltage Follower using a common-gate auxiliary amplifier. , 2016, , .		9
51	Calibration of pipeline ADC with pruned Volterra kernels. Electronics Letters, 2016, 52, 1370-1371.	0.5	4
52	Calibrating sample and hold stages with pruned Volterra kernels. Electronics Letters, 2015, 51, 2094-2096.	0.5	4
53	Design and validation through a frequency-based metric of a new countermeasure to protect nanometer ICs from side-channel attacks. Journal of Cryptographic Engineering, 2015, 5, 269-288.	1.5	15
54	Using feed array networks to control distortions in antenna reflector for astrophysical radio-astronomy. , 2014, , .		0

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55	Design of broad-band power amplifiers by means of an impedance transforming lossy equalizer. , 2014, , .		1
56	A wideband amplifier topology based on positive capacitive feedback. Microelectronics Journal, 2014, 45, 50-58.	1.1	2
57	An improved common-mode feedback loop for the differential-difference amplifier. Analog Integrated Circuits and Signal Processing, 2013, 74, 33-48.	0.9	6
58	Improved Digital Background Calibration of Time-Interleaved Pipeline A/D Converters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 86-90.	2.2	24
59	Efficient Digital Background Calibration of Time-Interleaved Pipeline Analog-to-Digital Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1373-1383.	3.5	38
60	An MDAC architecture with low sensitivity to finite opamp gain. , 2011, , .		0
61	A class-AB very low voltage amplifier and sample & hold circuit. , 2011, , .		0
62	A very low-voltage differential amplifier for opamp design. , 2011, , .		3
63	A class-AB flipped voltage follower output stage. , 2011, , .		19
64	Behavioral Modeling for Calibration of Pipeline Analog-To-Digital Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1255-1264.	3.5	24
65	Extraction of CADâ€compatible statistical nonlinear models of GaAs HEMT MMICs. Microwave and Optical Technology Letters, 2009, 51, 2163-2166.	0.9	0
66	A wideband high-CMRR single-ended to differential converter. Analog Integrated Circuits and Signal Processing, 2009, 59, 43-52.	0.9	1
67	Design Solutions for Sample-and-Hold Circuits in CMOS Nanometer Technologies. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 459-463.	2.2	28
68	Near-optimum switched capacitor sample-and-hold circuit. , 2009, , .		3
69	Switched Capacitor Sample-and-Hold Circuit with Input Signal Range beyond Supply Voltage. , 2008, , .		4
70	A low-power sample-and-hold circuit based on a switched-opamp technique. , 2008, , .		2
71	A Gain-Enhancing Technique for Very Low-Voltage Amplifiers. , 2008, , .		0
72	CMOS Miller OTA with Body-Biased Output Stage. , 2007, , .		3

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73	Power-constrained Bandwidth Optimization in Cascaded Open-loop Amplifiers. , 2007, , .		0
74	A Sample-and-Hold Circuit with Very Low Gain Error for Time Interleaving Applications. , 2007, , .		2
75	A High-Speed Low-Voltage Phase Detector for Clock Recovery From NRZ Data. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 1626-1635.	0.1	6
76	A Simple Technique for Fast Digital Background Calibration of A/D Converters. Eurasip Journal on Advances in Signal Processing, 2007, 2008, .	1.0	1
77	CMOS High-CMRR Current Output Stages. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 745-749.	2.3	13
78	A Statistical Model of Logic Gates for Monte Carlo Simulation Including On-Chip Variations. Lecture Notes in Computer Science, 2007, , 516-525.	1.0	2
79	Input-Matching and Offset-Cancelling Networks for Limiting Amplifiers in Optical Communication Systems. Analog Integrated Circuits and Signal Processing, 2006, 47, 23-32.	0.9	2
80	Analytic transient solution of SCFL logic gates. International Journal of Circuit Theory and Applications, 2005, 33, 365-378.	1.3	1
81	A Novel Dual-Output CCII-Based Single-Ended to Differential Converter. Analog Integrated Circuits and Signal Processing, 2005, 43, 87-90.	0.9	5
82	A 10-Gb/s CMU/CDR chip-set in SiGe BiCMOS commercial technology with multistandard capability. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 191-200.	2.1	4
83	An active balun for high-CMRR IC design. , 2005, , .		4
84	Behavioral model of a noisy VCO for efficient time-domain simulation. Microwave and Optical Technology Letters, 2004, 40, 352-355.	0.9	2
85	A new statistical model of nonlinear noisy oscillator. , 2004, , .		0
86	A new procedure for nonlinear statistical model extraction of GaAs FET-integrated circuits. International Journal of RF and Microwave Computer-Aided Engineering, 2003, 13, 348-356.	0.8	1
87	High-CMRR CMOS current output stage. Electronics Letters, 2003, 39, 945.	0.5	8
88	Model of flicker noise effects on phase noise in oscillators. , 2003, 5113, 424.		0
89	A bootstrap technique for wideband amplifiers. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2002, 49, 1474-1480.	0.1	22
90	A new model to analyze the effects of noise in a real oscillator. Microwave and Optical Technology Letters, 2002, 32, 305-307.	0.9	3

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91	A compact 3R-receiver module for short-haul SDH STM-16 systems. Journal of Lightwave Technology, 2001, 19, 1307-1315.	2.7	2
92	A bandwidth-compensated transimpedance amplifier for multigigabit optical receivers. Microwave and Optical Technology Letters, 2001, 30, 79-81.	0.9	2
93	A novel bias-dependent rational model for MESFET and HEMT devices. Microwave and Optical Technology Letters, 2000, 24, 102-106.	0.9	2
94	A new topology for a transimpedance amplifier with postfabrication bandwidth adjustment. Microwave and Optical Technology Letters, 2000, 25, 47-51.	0.9	2
95	Design of a transimpedance amplifier for 10 Gbit/s optical receivers with a new topology of active balun. Microwave and Optical Technology Letters, 2000, 27, 257-259.	0.9	1
96	A synthesis-oriented approach to design microwave multidevice amplifiers with a prefixed stability margin. , 2000, 10, 102-104.		9
97	A synthesis-oriented conditional stability criterion for microwave multidevice circuits with complex termination impedances. , 2000, 10, 460-462.		2
98	A low-power clock and data recovery circuit for 2.5 Gb/s SDH receivers. , 2000, , .		3
99	A novel topology for four-quadrant GaAs monolithic multipliers. Microwave and Optical Technology Letters, 1999, 21, 277-282.	0.9	0
100	<title>Monolithic 2.5-Gb/s clock and data recovery circuit based on silicon bipolar technology</title>. , 1998, , .		3
101	Input-matching and offset-compensation network for limiting amplifiers in optical communication systems. , 0, , .		1
102	A new topology of controlled C/sup 3/A differentiator for multi-Gb/s optical applications. , 0, , .		0
103	A tree-like amplifier architecture for large gain-bandwidth product. , 0, , .		0
104	Bipolar differential cell with improved bandwidth performance. , 0, , .		0
105	Current output stage with improved CMRR. , 0, , .		4
106	Robust three-state PFD architecture with enhanced frequency acquisition capabilities. , 0, , .		4
107	High-speed CMOS-to-ECL pad driver in 0.18Î¼m CMOS. , 0, , .		0
108	A model for the distortion due to switch on-resistance in sample-and-hold circuits. , 0, , .		10